T.E.: Sem 5 (Rev.)
P371 H KL-08/560
EXTC
Elements of Microelectronics. 03/06/0

Con. 3344-08. (REVISED COURSE) CO–2552

(3 Hours) [Total Marks : 100

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Assume **suitable** data, wherever **necessary**.

1. (a) Explain IC crossovers. 5
   (b) Define LSI, MSI and VLSI circuits. 5
   (c) Explain significance of lambda-based design rules for MOS–IC. 5
   (d) With the help of neat diagram explain important features of butting and buried contacts. 5

2. (a) Explain the following term's :— 10
      (i) Short channel effect
      (ii) Channel length modulation.
   (b) A MOS capacitor has an oxide thickness of 500A°. How much chip area is required to obtain a capacitance of 200 pf ? Assume E_r for S_i O_2 = 3·9. 5
   (c) Explain Rise time of EMD pull–up Inverter. 5

3. (a) Draw a circuit of CMOS inverter, explain its operation with the help of it's transfer characteristics. 10
   (b) Explain, what is partial scaling down and full scaling down MOS circuit. Give merits-demerits of such scaling operations. Does body effect of process limit the number of transistor's that can be placed in series in a CMOS gate at low frequencies. 10

4. (a) What is photolithography ? What are the different techniques involved in it ? Explain one of them in detail. 10
   (b) Draw stick diagram of end layout for 1 bit CMOS shif register cell. 10

5. (a) Discuss the parasitic effect's in MOSFETS. 10
   (b) What are the various crystal growth technics using in silicon industries ? Explain any one in brief. 10

6. (a) Compare a MOS transistor and Bipolar transistor from integrated circuits pointed of view. 10
   (b) Draw in detail the cross sectional view of FET capacitance. Derive expression for total capacitance of source and drain region of area 'A' and perimeter 'P'. 10

7. Write note on :— 20
      (a) Lateral PNP and vertical PNP transistor
      (b) The twin tub process
      (c) A MOS NAND gate
      (d) EDA tools used in VLSI Technology