B.E.–Exam.–09–300

B.E. (Comp) Sem VII (R) 30/05/09

Advanced Microprocessor

Con. 2872–09. VR–4746

(3 Hours) [Total Marks : 100

Lib 11 P.m to 2 P.m.

N.B. : (1) Question No. **1** is **compulsory**.

(2) Attempt any **four** questions out of remaining **six** questions.

1. (a) Differentiate between EISA and PCI bus. 5
   (b) Explain debug registers of X86 processors. 5
   (c) Explain the role of PDE and PTE in page translation mechanism. 5
   (d) Compare pentium-II xeon and celeron 5

2. (a) Draw the block diagram of the 80386 DX processor and explain each block in brief. 10
   (b) Compare super SPARC and ultra SPARC processors. Draw the architecture of super SPARC and explain. 10

3. (a) Explain the address translation mechanism in X86 processor. List all the steps in segment translation. 10
   (b) Draw and explain DEC Alpha AXP processor architecture — 21064. 10

4. (a) List the features of 8-bit and 16 bit ISA. Compare bus bandwidths of EISA, MCA and PCI bus. 10
   (b) Explain the following pentium-II instructions : 10
   CPUID, SYSENTER, SYSEXIT, FXSAVE, FXRSTOR.

5. (a) Draw and explain various instruction formats of SPARC processor. 10
   (b) Explain with block diagram, how superscalor operation is carried out in pentium processor. 10

6. (a) Draw the pentium-4 willamette architecture and explain in brief each block. 10
   (b) Draw the mode transition diagram of X86 processor and compare real and protected mode with respect to segment size, number of segments, page size, virtual memory support, addressing mechanism and interrupt processing. 10

7. Write short notes on :— 20
   (a) Aspects of segment level protection.
   (b) Internal data cache of pentium processor
   (c) Layered architecture of SCSI.
   (d) Pentium vs pentium pro-processor.