ME/ETRX/sem I 21/5/09

Microprocessor and sys. I

Con. 3227–09. BB–5667

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of **remaining** questions.

1. Design SBC with following specification :– **20**
   (a) 80386 DX operates at 25 MHz.
   (b) Firmware support of 128 KB using 32 KB EPROM devices.
   (c) Data memory support of 2 GB using 1 GB SRAM devices.
   (d) Two input and two output ports.
   Draw a neat diagram. Show memory and I/O maps.

2. Explain Trojan Horse attack. How operating system can prevent such an attack using ARPL instruction. **20**

3. Explain address translation mechanism of 80386 DX. Explain your answer for paging. **20**

4. (a) Cache coherancy problems and its prevention methods. Explain. **10**
   (b) Design one way and two way set associative cache organisation for the following case **10**
   – Main memory → 16 MB
   – Cache memory → 32 KB
   – Line size → 4 bytes
   Give the directory entry for both.

5. Explain the architecture of 80386 EX with a proper diagram. **20**

6. (a) Discuss the I/O protections of 80386 DX. **10**
   (b) Explain task switching for "Nested Task". **10**

7. (a) Explain ISA interrupt subsystem. **10**
   (b) Explain ISA timer. **10**