(Library) m. E. Sem-II. 22/5/09.

747 : H-m.

VLSI Design.

Con. 3230-09. **BB-5814**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any **suitable data** wherever **required** but **justify** the **same**.

1. (a) Find resistance Rn for nMOS if electron mobility $\mu_n = 560\ cm^2/V\text{-}sec$, $t_{0x} = 10$ nm, $\varepsilon_{0x} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}$ F/cm, and $V_G = 3{\cdot}3$ Volts, $V_{THn} = 0{\cdot}7$ Volts if $W = 10\ \mu m$, $L = 0{\cdot}5\ \mu m$. **20**
   (b) Determine intrinsic gate capacitance with $t_{0x} = 150\ A°$, $\varepsilon_{0x} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}$ F/cm, and $V_G = 3{\cdot}3$ Volts if $W = 4\ \mu m$ $L = 2\ \mu m$.
   (c) Explain **Sa'0'** and **Sa'1'** fault modeling with respect to 2-i/p NAND gate.
   (d) With proper diagram explain an inverting type supper-buffer also explain the need of supper-buffer.
   (e) Explain different types of contacts in case of nMOS depletion type of device. State their limitations and advantages.

2. (a) Explain with suitable diagram the band bending in case of MOS capacitor. Clearly state all the three phases in case of nMOS capacitor. **10**
   (b) Derive expression for the drain current in nMOS device in both regions of operation (linear and saturation region) also explain what do you mean by channel length modulation. **10**

3. (a) Explain what body bais effect is. Derive expression for the Threshold shift and also explain the effect of body bais on performance of the device in following example— **10**
   Where $V_{SB} = 1{\cdot}5$ Volts, $N_A = 3 \times 10^{16}\ cm^{-3}$, $t_{0x} = 300°A$, $\varepsilon_0 = 8{\cdot}85 \times 10^{-14}$ F/cm
   $\varepsilon_{0x} = 3.9\ \varepsilon_0$, $\varepsilon_{si} = 11{\cdot}7\ \varepsilon_0$, $n_i = 1{\cdot}5 \times 10^{10}\ cm^{-3}$, $q = 1{\cdot}6 \times 10^{-19}$ C
   (b) In an Inverter what do you mean by Inverter Ratio ? Determine the Inverter Ratio for a depletion load nMOS Inverter which is driven by another same type of Inverter. **10**

4. (a) Derive an expression for V_{IL}, V_{IH}, V_{OH} and V_{OL} for CMOS Inverter with respect to its transfer characteristics. **10**
   (b) Explain switching characteristics of CMOS Inverter and explain how to determine the rise and fall time for the capacitive load CL also how to make the switching symmetrical ? **10**

5. (a) Make a stick diagram, schematic and Euler path for **10**
   $Y = \overline{a(b + c)}$
   Also draw layout for the same.
   (b) Draw the schematic of 4-i/p and 4-o/p Barrel Shifter using nMOS. **10**

6. (a) Discuss the limitation of scaling of MOS device. How do the following parameters changes after scaling ? **10**
      (i) Gate Delay
      (ii) Power Dissipation
      (iii) Device trans-conductance.
   (b) Describe the importance of oxide film in integrated circuit fabrication. Explain various methods to evaluate the quality of oxide film grown on silicon wafer explain their merits and limitations. **10**

7. Write a short notes on (any **four**) :— 20

(a) Bi-CMOS
(b) Domino Logic
(c) Design rules and its significance
(d) Fick's Law Governing Diffusion
(e) Latch-up problem in CMOS
(f) Drain-punchthrough.