S.E. (Com) Sem III (R) 03/06/09

Con. 2874-09. Computer Organization & Architecture **VR-3324**

(REVISED COURSE)

(Li6)

3 p.m to 6 p.m.

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions out of **remaining**.
(3) Draw **neat labeled diagram** wherever **necessary**.

1. (a) Explain with suitable examples the difference between computer architecture and computer organization. **5**

   (b) Define the following terms : **5**
   (i) Memory Access Time (MAT)
   (ii) Memory Cycle Time (MCT)
   (iii) Spatial locality of reference
   (iv) Temporal locality of reference
   (v) Cache block.

   (c) Explain IEEE format for floating point number representation. **10**

2. (a) Explain and solve the following problem using by restoring division algorithm ? Hence divide $(163)_{10}$ **with** $(11)_{10}$. **10**

   (b) A 32- bit computer has a 32 bit memory address. It has 8 KB of cache memory. The computer follows four-way set associative mapping. Each line size is 16 bytes. Show the memory address format and cache memory organization. **10**

3. (a) What is memory interleaving ? Discuss various memory interleaving techniques. **10**

   (b) Explain the general organization of CPU ? State the function of following CPU registers. **10**
   (i) MAR (Memory Address Register)
   (ii) MDR (Memory Data Register)
   (iii) IR (Instruction Register)
   (iv) PC (Program Counter)
   (v) SP (Stack Pointer).

4. (a) What is Virtual memory ? Explain how paging is useful in implementing virtual memory ? **10**

   (b) Define "(Input/Output) I/O Module ?" State the difference between programmable and non-programmable device ? Explain in brief DMA data transfer techniques with diagram. **10**

5. (a) Define the term "softwired" and "hardwired" . Explain nano-programming. **10**

   (b) What is "Micro program" ? Write a Micro program using RTL (register transfer language) notation for the following arithmetic operation. **10**

   (i) SUB Rl,R2 i.e Rl ← Rl - R2

   (ii) MUL Rl,R2 i.e Rl ← Rl*R2

6. (a) Explain in brief about SPARC processor ? Draw and explain in brief n-bit windows architecture of SPARC processor ? **10**

   (b) Explain the Flynn's Classification in detail ? **10**

7. (a) What is pipelining ? Show that K stage pipe lined processor has K times speed up compared to a non pipe lined systems. **10**

   (b) Explain wave front array with suitable example ? **10**