S.E. (EXTC) Sem III (R) 20-5-09

Con. 2634–09. (REVISED COURSE) VR–3363

(3 Hours) [Total Marks : 100

Digital Logic Design 3 p.m. to 6 p.m.

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** out of remaining **six**.
(3) Figures to the **right** indicate **full** marks.
(4) Assume **suitable** data if **required**.

1. (a) Find 2's compliment for the given binary number. **2**
   (i) 0·0101 (ii) 1101·01
   (b) Perform the following subtraction by using g's compliments method. **3**
   (i) 5240–76532 (ii) 76532–4250
   (c) Write the comparision between 1's compliement and 2's compliment. **2**
   (d) Explain in brief Hamming code **2**
   (e) Solve the equation for x **2**
   $(x)_{16}$ = 1111 1111 1111 1111
   (f) Express the following decimals in Gray code form **3**
   (i) 42 (ii) 340
   (g) What are the advantages of digital system ? **3**
   (h) What is BCD code ? What are its advantages & disadvantages. **3**

2. (a) Design a combinational logic circuit that has four inputs and one output. The output is equal to 1 when an input have above 1000. **10**
   (b) Design Excess–3 to BCD code converter. **10**

3. (a) Given the logic function $f = ABC + B\bar{C}D + \bar{A}BC$ **10**
   (i) Make a truth table
   (ii) Simplicity using a k-map
   (iii) Realise f using NAND Gates only.
   (b) Explain the following laws of boolean algebra and prove them using truth tables. **10**
   (i) Associative Law (iv) Absorption Law
   (ii) Distributive Law (v) Idempotency
   (iii) Commutative Law

4. (a) Deine propagation Delay ? What is fan-in and fan-out ? What is meant by power dissipation ? What is Noise Margin ? Explain with suitable examples. **10**
   (b) Explain the following boolean equation using 8 : 1 MUX. **10**
   F (A, B, C, D) = Σm (o, 1, 3, 4, 8, 9, 15)

5. (a) Implement the full adder with a decoder circuit. **6**
   (b) Design BeD to 7-segment decoder and realize the circuit. **8**
   (c) Use a MUX to generate the function. **6**
   $F = \bar{A}B\bar{C} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D$.

6. (a) Explain the process of JK flipflop to SR flip-flop conversion. **10**
   (b) Explain universal thift Register. **10**

7. (a) Differentiate between synchronous and Asynchronous counter. **4**
   (b) Design MOD-5 counter using JK flipflop and implement it. **8**
   (c) Design a counter for the following sequence. **8**
   1, 2, 5 and 7 .....