S.E. (E&T.C.) Sem III (R) 25-5-09

P4–Exam.–09–206

Digital logic design & Application 3 pm to 6 pm

Con. 2512–09. (REVISED COURSE) VR–3399

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** additional data if **required**.

1. (a) State Demorgan's theorem and Implement EX-OR gate using NAND gates only. 4
   (b) Perform the following operations without converting to any other base :– 4
      (i) $(63)_8 \times (21)_8$
      (ii) $(2Fg)_{16} - (1AD)_{16}$.
   (c) Obtain 7 bit Even parity Hamming code for the data (1101). Why Hamming code is an error detecting code ? 4
   (d) Implement given equations using 2 : 1 multiplexer :– 4
      (i) $y = A + B$
      (ii) $y = AB$
   (e) Convert T Flipflop into D Flipflop. 4

2. (a) Given the Logic expression :– 10

   $Y = A + \overline{B}\,\overline{C} + AB\overline{D} + ABCD$

      (i) Express it in standard SOP form
      (ii) Draw k-map and simplify
      (iii) Draw Logic diagram using NAND gates only.
   (b) Design 2 bit digital comparator using minimum number of gates. 10

3. (a) Minimise the following Boolean function by using Quine-Mccluskey tabular method. 10
      $F(A, B, C, D) = \Sigma_m (0, 2, 3, 6, 7, 8, 10, 12, 13)$
   (b) Implement BCD adder using 4 bit binary adder IC 7483. Explain its operation by adding 0101 and 0110. 10

4. (a) Draw the Logic diagram of JK Flipflop using NAND gates and explain its operation and write its truthtable, excitation table and derive an expression for the next state. 10
   (b) Explain the essential features of VHDL and wirte a VHDL program for full adder. 10

5. (a) Design a Mod 10 asynchronous counter using T Flipflop. What is glitch problem ? How do you remove the glitch ? 10
   (b) Design full substructure circuit using PAL and PLA. 10

6. (a) Design a synchronous counter for the following sequence using D Flipflop. 10
      2 – 6 – 5 – 3 – 1 – 0 – 2
   (b) What is a carry look ahead adder ? Design a 4 bit carry look ahead adder using gates. 10

7. Write short notes on any **two** :– 20

(a) Mealy and Moore machines

(b) Bidirectional shift register

(c) Priority encoder

(d) CAD Tools.