

Con. 2983-09.

VR-3759

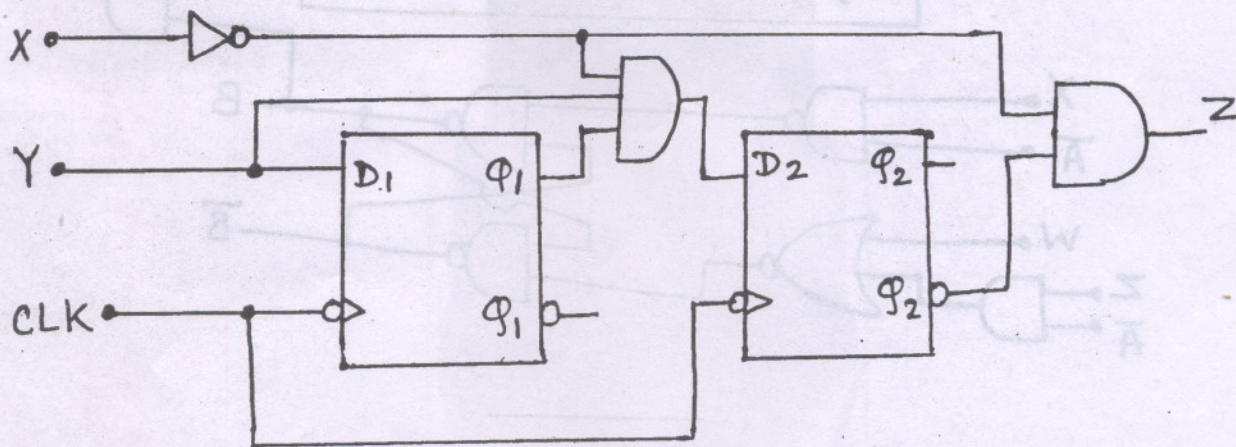
(REVISED COURSE)

(3 Hours)

[Total Marks : 100

- N.B.: (1) Question No. 1 is compulsory.  
 (2) Attempt any **four** questions out of remaining **six** questions.  
 (3) Assume any **suitable** data wherever **required** but justify the **same**.  
 (4) **Figures** to the **right** indicate marks.

1. (a) Write VHDL Code for JKFF having asynchronous preset and clear terminals. **5**  
 (b) Draw a state diagram for single I/P, single O/P Mealy machine to detect two sequences 1010 and 0101. Both the sequences are overlapping. **5**  
 (c) Explain the analog controls available in I/O block of XC 4000 FPGA family. **5**  
 (d) Compare the synchronous and Asynchronous sequential machines. **5**
2. (a) Listout different Modeling styles in VHDL. Using any one modeling style, write VHDL code for 5 bit even and odd parity generator circuit. **10**  
 (b) Write VHDL code for Floating point Encoder, considering 11 bit data and 4 Bit Mantissa. Is it a sequential circuit ? **10**
3. (a) Write VHDL code for 2 digit BCD counter. **10**  
 (b) Write VHDL program for 16:1 MUX. Use only concurrent statements and 4:1 MUX as a component. **10**
4. (a) Analyse the sequential machine shown, and obtain the state diagram. **10**



- (b) Reduce the state table using Implication chart method and design state machine using DFF. Use decoders for generation of excitation inputs. **10**

Present State	Next State			
	X = 0	Z	X = 1	Z
S0	S4	0	S3	1
S1	S5	0	S3	0
S2	S4	0	S1	1
S3	S5	0	S1	0
S4	S2	0	S5	1
S5	S1	0	S2	0

5. (a) A clocked mealy sequential network should have an output  $Z = 1$ , if the total number of zeros received is an even number greater than zero, provided that two consecutive one's have never been received. Design the machine using minimum risk approach of design and TFF. 10
- (b) Write VHDL Code for state table given in Q. 4(b). Make use of "Process" statement. 10
6. (a) Draw and explain the working of SRAM cell. Using it, draw the structure for  $4 \times 2$  SRAM Memory unit. 10
- (b) With reference to XC 9500 CPLD family explain : 10
  - (i) Architecture of functional block
  - (ii) Product term Allocator and Macrocell structure.
7. (a) Design Mod—193 counter with the counting sequence 63—64 — . . . . . 254 — 255 — 63—64, using IC 74 x 169. 10
- (b) Analyse the pulse mode asynchronous sequential machine and obtain the state diagram. 10

