

(REVISED COURSE)

(3 Hours)

[Total Marks : 100

- N.B. : (1) Question No.1 is compulsory.  
 (2) Answer any four questions from remaining.  
 (3) Assume suitable data wherever necessary.  
 (4) Draw neat circuit diagram wherever necessary.

1. (a) Give the difference in frequency response of integrator and Low-pass filter. 4  
 (b) Find  $V_N$ ,  $V_P$  and  $V_O$  in the circuit of figure 1(b). 4

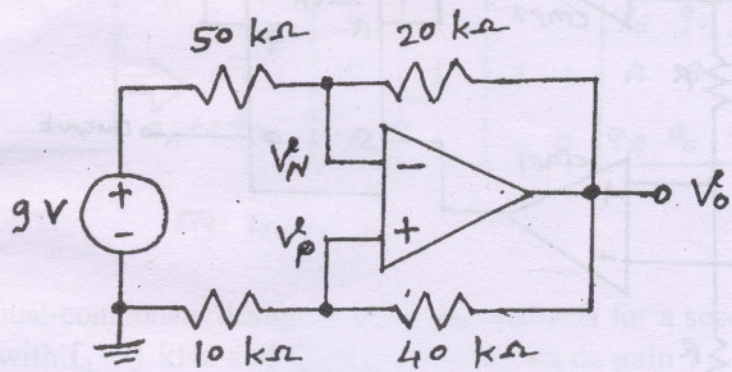


Fig. 1(b)

- (c) With neat circuit explain any one technique of A-to-D conversion. 4  
 (d) Give the difference between Moore machine and Mealy machine. 4  
 (e) Give the difference between FPGAs and CPLDs. 4

2. (a) Define voltage-to-current converter. 2  
 Determine the condition under which the circuit shown in figure 2(a) can work as voltage-to-current converter. 8

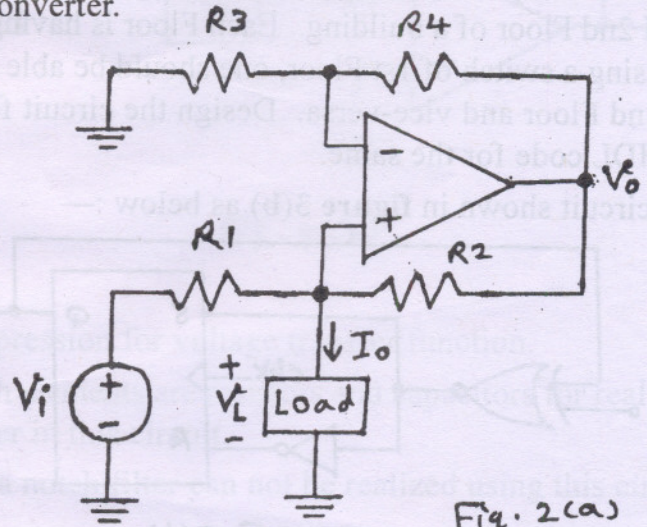


Fig. 2(a)

(b) Analyse the circuit shown in figure 2(b) as below :—

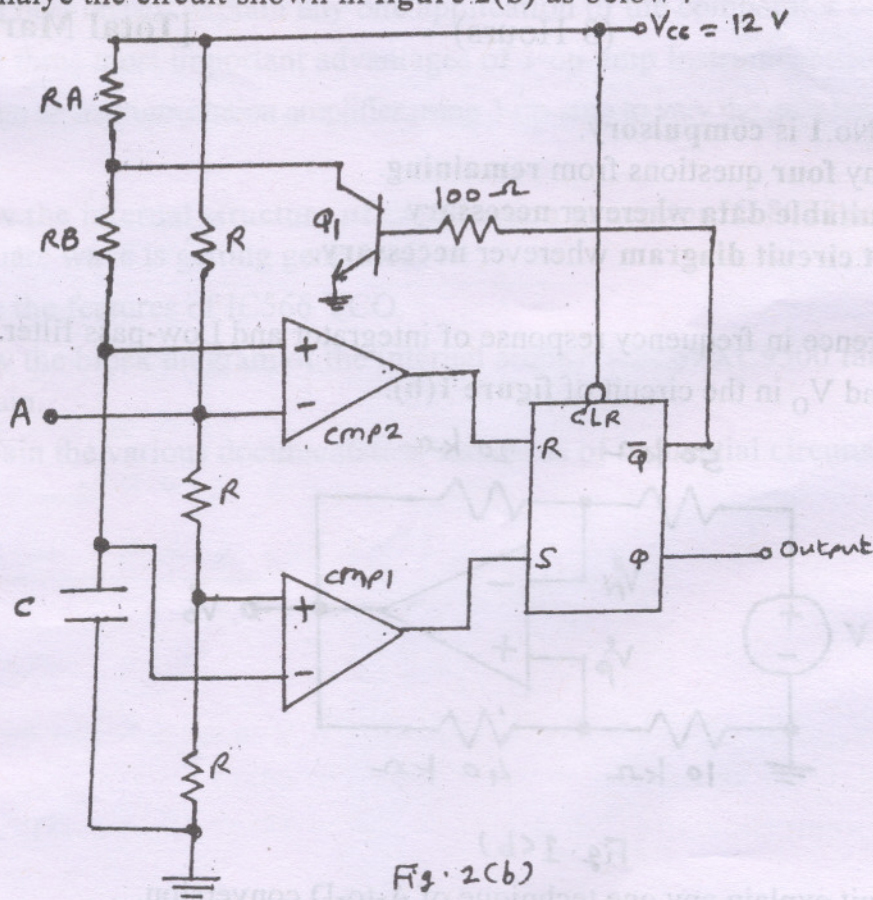


Fig. 2(b)

- (i) Explain the working of the circuit. 4
- (ii) Draw the waveform seen at the output and across capacitor. 4
- (iii) Explain whether the output frequency will increase, decrease or remains same if the 8 V dc is applied at node A. 2

3. (a) It is desired to develop the circuit for controlling a lamp on the staircase between 1st Floor and 2nd Floor of a building. Each Floor is having a switch. if a lamp is made 'ON' using a switch of 1st Floor, one should be able to make it 'OFF' using a switch of 2nd Floor and vice-versa. Design the circuit for the same. Write the VHDL code for the same. 5

(b) Analyse the circuit shown in figure 3(b) as below :—

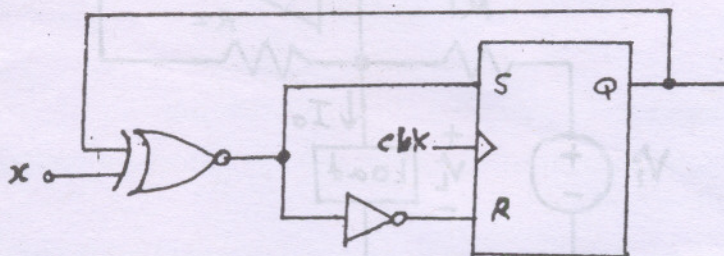


Fig. 3(b)

- (i) Construct the transition table. 4
- (ii) Construct the state table. 4
- (iii) Draw its state diagram. 2

4. (a) Write the VHDL code for synchronous decade counter with rising clock edge and asynchronous clear input. 10
- (b) IC 74 x 194 is a 4-bit universal shift register. Its logic symbol and the functionality is given in figure 4 (b). Design a 4-bit Johnson counter using IC 74 x 194. 5
- Draw its timing diagram. 5

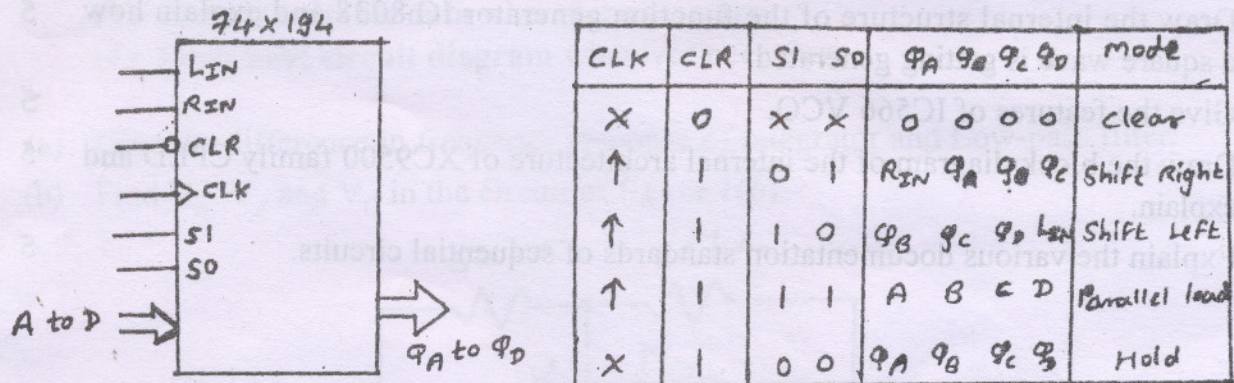


Fig. 4 (b)

5. (a) Using the equal-component design, specify the elements for a second-order low-pass KRC filter with  $f_0 = 1$  kHz and  $Q_0 = 5$ . What is its dc gain? 10
- (b) Analyse the circuit shown in figure 5(b) as below where all 'Ys' represents admittances.

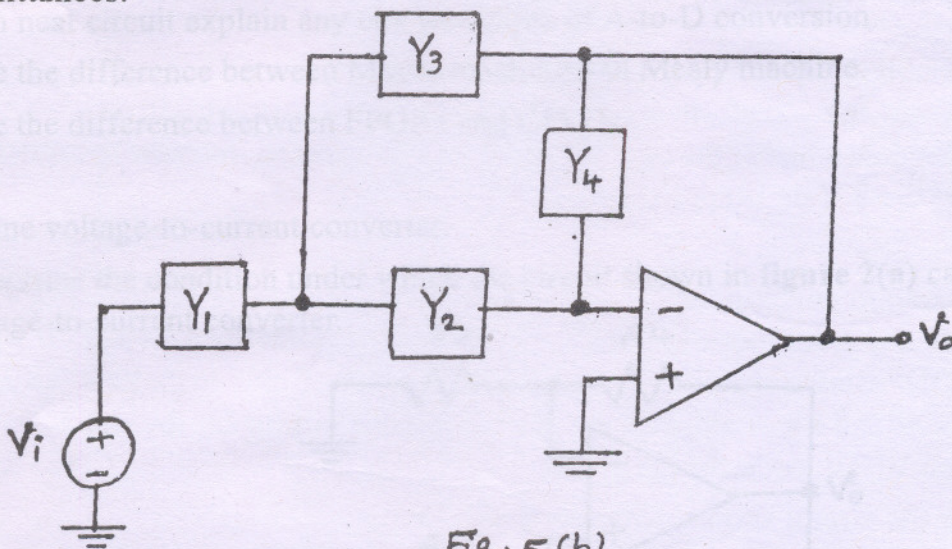


Fig. 5 (b)

- (i) Derive the expression for voltage transfer function. 5
- (ii) Identify, which elements are resistors and capacitors for realizing active RC band-pass filter in this circuit. 3
- (iii) Explain, why a notch filter can not be realized using this circuit? 2

6. (a) Differentiate between static RAM and dynamic RAM. 5
- (b) With neat circuit explain any one application of the comparator circuit. 5
- (c) Give three most important advantages of 3-op-amp Instrumentation amplifier. 3
- Design an Instrumentation amplifier using 3-op-amp to vary the gain between 0.5 to 500. 7
7. (a) Draw the internal structure of the function generator IC 8038 and explain how a square wave is getting generated. 5
- (b) Give the features of IC566 VCO. 5
- (c) Draw the block diagram of the internal architecture of XC9500 family CPLD and explain. 5
- (d) Explain the various documentation standards of sequential circuits. 5