TE (EXTC) V (R)
Elements of Microelectronics
01/06/09
3-6 p.m.

Con. 2964–09. (REVISED COURSE) VR–5160

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.

1. (a) Give merits and demerits of MOS Integrated Circuits. **5**
   (b) Define LSI, MSI, VLSI and ULSI Circuits. **5**
   (c) Discuss fabrication density, system speed, power dissipation and their inter-dependence in detail. **5**
   (d) Explain MOSFET operation. **5**

2. (a) What are the various crystal growth techniques used in silicon industries ? Explain any one in brief. **10**
   (b) With neat diagram explain the fabrication sequence of CMOS Inverter using N-well process. **10**

3. (a) Describe the formation of resistors in integrated circuit. How will you optimize the design ? **10**
   (b) What are different types of scaling ? Explain their advantages and disadvantages. **10**

4. (a) What is the minimum number of isolation regions required to realize in monolithic form for 2 input. TTL NAND Gate. Draw monolithic layout of this gate ? **10**
   (b) Explain different short channel effects in MOSFET. **10**

5. (a) Explain the need of design rules and explain significance of λ based design rules. **10**
   (b) Calculate the threshold voltage V_{TO} for a polysilicon gate n-channel MOS transistor, with the following parameters : **10**
   Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500A°$, and oxide - interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}.
   (Data $\frac{kT}{q} = 26$ mV, $\epsilon_o = 8{\cdot}85 \times 10^{-14}$ F/cm, $K_{ox} = 3{\cdot}9$, $n_i = 1{\cdot}45 \times 10^{10}$ cm^{-3}, $k_{si} = 11{\cdot}7$)

6. (a) Design CMOS logic gates for the following function. **10**
   (i) $Z = \overline{(A + B)\ (C + D)}$
   (ii) $Z = \overline{A\ (B + C) + CD}$
   (b) Discuss different parasitic effects in MOS transistors. **10**

7. Write short notes on the following :— **20**
   (a) Butting and Buried contacts
   (b) CMOS Latchup
   (c) BJT Fabrication
   (d) IC Cross Overs.