Con. 3079-09. (REVISED COURSE) VR-5307

T.E. CETRX) Sem II (CR) 23-5-09

(3 Hours) [Total Marks : 100

Computer Organisation 3p.m. to 6.p.m.

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from Question Nos. **2** to **7.**
(3) **Figures** to the **right** indicates **full** marks.

1. (a) Show direct mapping for following memory structure :— **10**
   Cache size = 32 words
   Main memory = 128 words
   Show detail structure.
   (b) Compare paging and segmentation in brief. **5**
   (c) Solve using Non-Restoring Division Method 12/5. **5**

2. (a) Analyze 2 level memory hierarchy with specification given below :— **10**

Level → / Parameter ↓	Cache (M1)	Main memory (M2)
Size	1 kb	64 kb
Cost/Byte	0·5	0·05
Access time	10 nsec	100 nsec

Calculate :
(i) Average cost/byte
(ii) Average access time
(iii) Efficiency.

(b) What is the necessity of replacement algorithm show how pages are replaced using following policies ? **10**
(i) LRU (ii) FIFO (iii) LFU find hit ratio.
Pages in main memory — 2 1 2 3 1 5 4 2 1 5
Pages In cache memory — 3 pages

3. (a) What is microprogramming ? Draw schematic of micro programmed Control unit. **10**
   (b) Draw schematic of Single Bus organization and write micro operation for following instruction for the same :— **10**
   (i) Mov Rd, Rs
   (ii) ADD R1, [R2]

4. (a) How is a page In memory accessed ? What is a TLB ? **10**
   (b) Explain data hazards in a linear pipelining system and prove that for a K stage Pipeline. The speed up factor = K. **10**

5. (a) Explains I/O accessing techniques in details with advantage and disadvantage. **10**
   (b) Explain various step taken by a CPU in interrupt processing. Explain how multiple devices. Share a single interrupt line. **10**

6. (a) Explain various DMA transfer Modes in brief with suitable example. **10**
   (b) Explain concept of cache memory with reference to principle of locality of Reference, Hit ratio and different cache architectures. **10**

7. (a) Explain various cache issue in multiprocessor systems. **10**
   (b) Explain various performance measures of CPU and techniques to enhance those. **10**