

Con. 3326-10.

(REVISED COURSE)

AN-3424

(3 Hours)

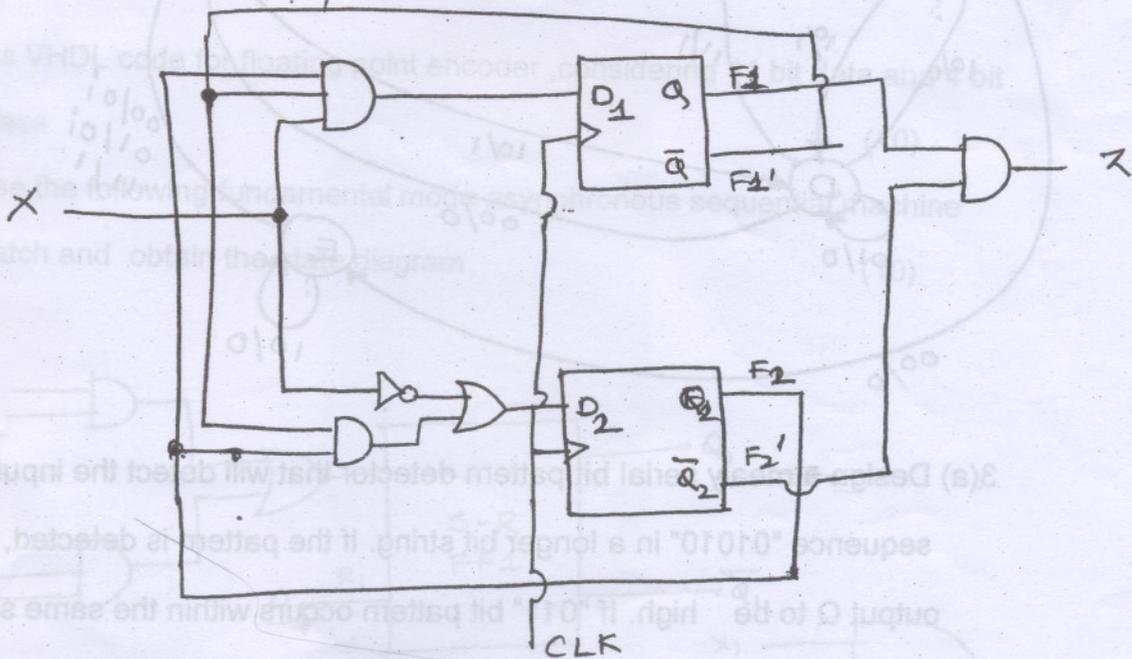
[Total Marks : 100

- N.B. : (1) Question No. 1 is compulsory.  
(2) Attempt any four from the remaining.  
(3) Make suitable assumptions if necessary.

1.a) Analyze the sequential machine and draw state diagram. (Use state named

A - D for  $F_1F_2 = 00 - 11$ . Clearly show all the steps.

(10)



b) Write a VHDL code for 4 bit asynchronous counter using T FF. Use

(10)

structural modeling.

2.a) Design a modulo-16 counter using 74169 and SSI package, with the

(10)

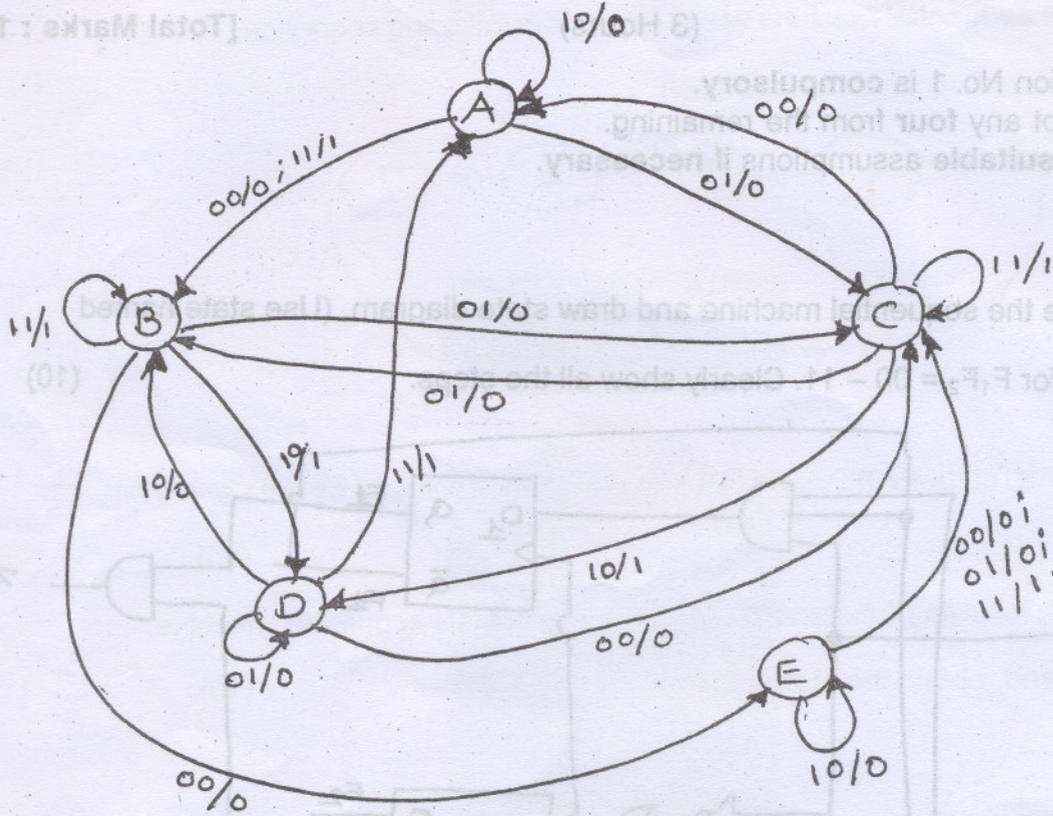
following counting sequence ....7,6,5,4,3,2,1,0,8,9,10,11,12,13,14,15,7,6,....

Explain the logic used.

b) Consider the state diagram in the figure shown. Determine any redundant

states and reduce the diagram if any.

(10)



3(a) Design a mealy serial bit pattern detector that will detect the input (10)

sequence "01010" in a longer bit string. If the pattern is detected, cause output Q to be high. If "011" bit pattern occurs within the same serial data string, cause output P to be high. Occurrence of 011 pattern cause the state machine to initialize. Overlapping of 01010 pattern can occur. Use decoders for excitation inputs.

b) Write VHDL code for IC 74163. Include all features. (10)

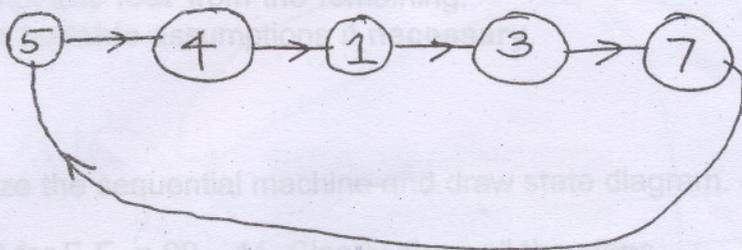
4.a) Design a coin operated vending machine that dispenses candy under the following conditions. (10)

- (i) The machine accepts Rs.5 and Ra.10 coins.
- (ii) It takes Rs.15 for one piece of candy to be released from the machine
- (iii) If Rs.20 is deposited the machine will credit the buyer with Rs.5 and wait for the buyer to make second purchase.

b) Draw the state diagram for the following moore machine and write VHDL code for the same. The state machine detects three or more consecutive 1's in string of bits coming through an input line. (10)

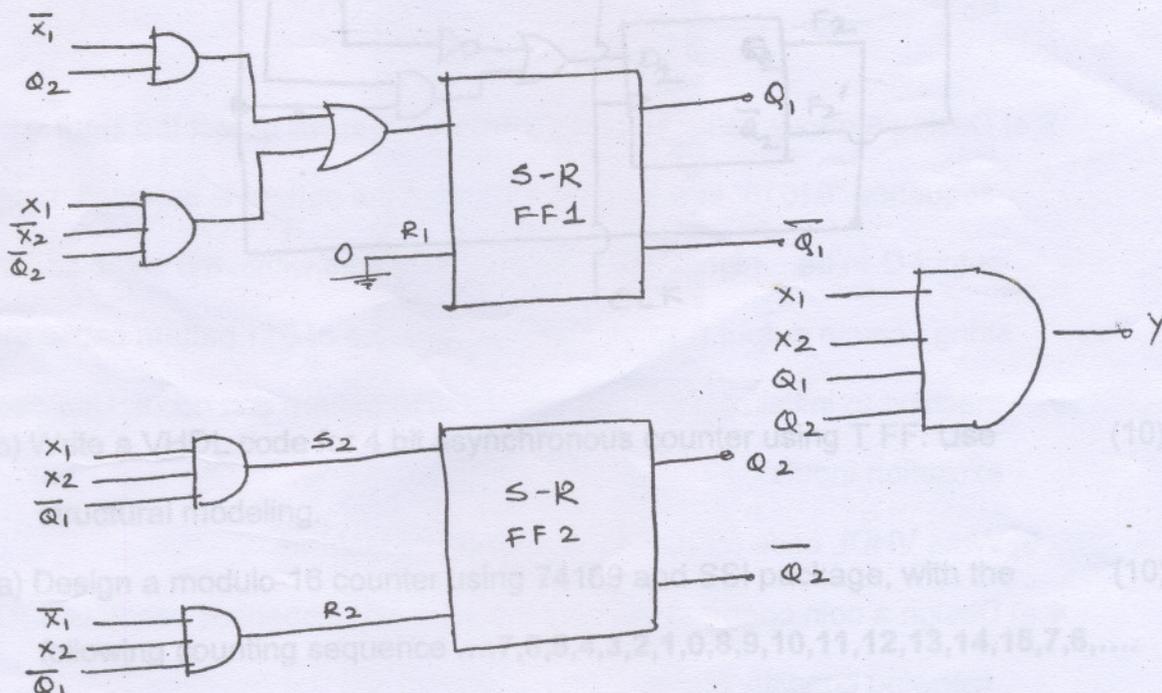
5.a) Design the sequential machine which counts the following sequence. (10)

Use JK FF and minimal risk approach



b) Write a VHDL code for floating point encoder, considering 11 bit data and 4 bit mantissa (10)

6.a) Analyse the following fundamental mode asynchronous sequential machine with latch and obtain the state diagram. (10)



b) Write a VHDL code for JK FF. Use asynchronous PRESET and synchronous CLEAR (10)

7.a) With reference to XC9500 CPLD Family explain (10)

- (i) Architecture of functional block (10)
- (ii) Product term allocator and macro cell structure.

b) Draw and explain logic diagram of 64 X 1 diode. Use two dimensional decoding. (10)

(3 Hours)

[ Total Marks : 100

**N.B.** (1) Question No. 1 is compulsory.

(2) Answer any four questions out of the remaining six questions.

(3) Figure to the right indicate full marks.

1. (a) The length of time (in minutes) a lady speaks on telephone is found to be a random variable with probability density function :

$$f(x) = Ae^{-x/5} \quad \text{for } x \geq 0 \\ = 0 \quad \text{otherwise.}$$

Find the value of A and the probability that she will speak for :—

- (i) more than 10 minutes  
(ii) less than 5 minutes.

- (b) A relation R in the set of integers is defined by  $xRy$  if and only if  $x < y + 1$ . Examine whether R is :—

- (i) reflexive  
(ii) symmetric  
(iii) transitive.

- (c) Find the eigen values of  $A^2 - 2A + I$  where :

$$A = \begin{bmatrix} 2 & 3 & 4 \\ 0 & 4 & 2 \\ 0 & 0 & 3 \end{bmatrix}$$

- (d) Find Taylor's series expansion of  $f(z) = \frac{1}{z^2 + 4}$  about  $z = -i$ .

2. (a) Seven coins are tossed and the number of heads obtained is recorded. The experiment is repeated 128 times and the following distribution is obtained :—

|              |   |   |    |    |    |    |   |   |
|--------------|---|---|----|----|----|----|---|---|
| No. of heads | 0 | 1 | 2  | 3  | 4  | 5  | 6 | 7 |
| Frequency    | 7 | 6 | 19 | 35 | 30 | 23 | 7 | 1 |

Fit a Binomial distribution if :—

- (i) The coins are unbiased  
(ii) If the nature of the coins is not known.

- (b) Using Residue theorem evaluate :

$$\int_C \frac{(z+4)^2}{z^4 + 5z^3 + 6z^2} dz \quad \text{where } C \text{ is the circle } |z| = 1.$$

- (c) Prove that the set of fourth roots of unity  $G = \{1, -1, i, -i\}$  is an abelian group under multiplication of complex numbers.

3. (a) Show that  $R = \{ 0, 2, 4, 6, 8 \}$  is a ring under addition and multiplication modulo 10. Is it an integral domain? Is it field? 7

(b) A die was thrown 132 times and the following frequencies were noted :— 7

|                                      |    |    |    |    |    |    |
|--------------------------------------|----|----|----|----|----|----|
| <b>Number obtained on upper face</b> | 1  | 2  | 3  | 4  | 5  | 6  |
| <b>Frequency</b>                     | 15 | 20 | 25 | 15 | 29 | 28 |

Test the hypothesis that the die is unbiased.

(c) Sum of eigen values of  $3 \times 3$  matrix is 6 and the product of eigen value is also 6. If one of the eigen value is 1, find other two eigen values. Clearly state the results which you use. 6

[ TURN OVER

4. (a) State moment generating function for Binomial distribution and hence find its mean and variance. 7
- (b) If the heights of 500 students is normally distributed with mean 68 inches and standard deviation 4 inches, estimate the number of students having heights :— 7
- (i) greater than 72 inches
- (ii) between 65 and 71 inches.
- (c)  $f : \mathbb{R} \rightarrow \mathbb{R}$  defined as  $f(x) = x^2$ ,  $g : \mathbb{R} \rightarrow \mathbb{R}$  is defined as  $g(x) = 3x + 7$ , find expressions defining :— 6
- (i) fog (ii) gof (iii) gog.
5. (a) After correcting 50 pages of the proof of a book, the reader finds that there are on the average 2 errors per 5 pages. How many pages would one expect to find, 0, 1, 2 and 3 errors in 1000 pages of first print of the book ? 7

- (b) Determine whether the matrix  $A = \begin{bmatrix} 1 & -6 & -4 \\ 0 & 4 & 2 \\ 0 & -6 & -3 \end{bmatrix}$  is similar to diagonal matrix. 7

- (c) Determine the nature of poles of the following function, also find the residue at each pole : 6

$$f(z) = \frac{\sin \pi z}{(z-1)^2 (z-2)}.$$

6. (a) A tyre company claims that the lives of tyres have mean 42000 km with standard deviation 4000 kms. A change in production process is believed to result in better product. A test sample of 81 new tyres has mean life of 42500 kms. Test at 5% LOS that the new product is significantly better than the old one. 7
- (b) Let  $A = \{ 2, 3, 6, 12, 24, 36 \}$  and  $R$  be the relation 'is divisible by' that is,  $a R b$  mean  $a$  divides  $b$  obtain relation matrix and Hasse diagram. 7
- (c) If  $X_1$  has mean 5 and variance 5,  $X_2$  has mean  $-2$  and variance 3. If  $X_1$  and  $X_2$  are independent random variables, find :— 6
- (i)  $E(X_1 + X_2)$ ,  $V(X_1 + X_2)$
- (ii)  $E(2X_1 + 3X_2 - 5)$ ,  $V(2X_1 + 3X_2 - 5)$ .

7. (a) A random variable X has the following probability distribution :—

7

|                  |     |     |     |
|------------------|-----|-----|-----|
| <b>X</b>         | -2  | 3   | 1   |
| <b>P (X = x)</b> | 1/3 | 1/2 | 1/6 |

Find :—

- (i) Moment generating function
- (ii) First two raw moments
- (iii) First two central moments.

(b) Verify Cayley-Hamilton theorem for the following and hence find  $A^{-1}$ , where :

7

$$A = \begin{bmatrix} 7 & -1 & 3 \\ 6 & 1 & 4 \\ 2 & 4 & 8 \end{bmatrix}$$

(c) Evaluate  $\int_C \frac{\sin^6 z}{\left(z - \frac{\pi}{6}\right)^3} dz$  where C is  $|z| = 1$ .

6

15 June 2010

S.E. EX-22 / sem IV / Rev  
E and E M I and M.

(ETRA)

VT-April-10-184

Con. 3809-10.

(REVISED COURSE)

AN-3436

Electronic & Electrical measuring Instruments & machine

(3 Hours)

[ Total Marks : 100

N.B. : (1) Question No. 1 is compulsory.

(2) Attempt any four questions out of remaining six questions.

(3) Assume suitable data wherever required and state clearly.

(4) Figures to the right indicate full marks.

1. Answer any four of the following :- 20
  - (a) What are the advantages of electronic voltmeter over the other voltmeters ?
  - (b) State the advantages, disadvantages and errors in PMMC instrument ?
  - (c) Explain the applications and the limitations of the wheatstone bridge.
  - (d) Explain the working principle of DC motor.
  - (e) Explain the method of Lissajous patterns used for the frequency measurement.
  
2. (a) Explain the R/2R ladder technique of D to A conversion. 10  
 (b) Explain the various performance parameters of digital voltmeter. 10
  
3. (a) Explain the digital frequency meter with neat diagram. 10  
 (b) Explain digital phase meter using flip/flop. Write its advantages and disadvantages. 10
  
4. (a) Explain beat frequency oscillator and its advantages. 10  
 (b) Draw and explain the block diagram of digital storage oscilloscope. 10
  
5. (a) An energy meter is designed to make 100 revolutions of the disc for one unit of energy. Calculate the no of revolutions made by it when connected to a load carrying 20 A, at 230 V, at 0.8 p.f. for an hour. If it makes 360 revolutions actually, find the % error. 10  
 (b) Derive the torque equation for moving iron instruments. 10
  
6. (a) Which measurements can be carried out by Maxwell bridge ? Derive the balance equation and expressions for the unknown components. 10  
 (b) Explain the operating principle of 3-phase induction motor. 10
  
7. Write short note on any three of the following :- 20
  - (a) Stepper motor
  - (b) Megger
  - (c) FET Voltmeters
  - (d) Use of CRO in component testing.

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5 June 2010

S.E. ETRXS Sem IV Rev

VT-April-10-146

Basic of Analog & Digital Communication  
(REVISED COURSE) AN-3427 System

Con. 3594-10.

( 3 Hours )

[ Total Marks : 100

- N.B. :** (1) Question No. 1 is **compulsory**.  
(2) Attempt any **four** questions from remaining **six** questions.  
(3) Assume **suitable** data wherever **necessary**.  
(4) **Figures** to the **right** indicate **full** marks.  
(5) **Illustrate** answers with **sketches** wherever **required**.

1. Attempt any **four** of the following :- 20
- (a) Classify and explain to various noises that affect communication.
  - (b) DSB-FC (A.M.) is wastage of power and bandwidth. Justify.
  - (c) Derive the expression for A.M.
  - (d) Explain the following characteristics of radio receiver :-
    - (i) Sensitivity
    - (ii) Selectivity
    - (iii) Fidelity
    - (iv) Double spotting
    - (v) Image frequency and its rejection.
  - (e) Explain companding and its need in communication.
2. (a) Explain basic block diagram of communication in detail. 6  
(b) Explain the following terms :- 8
  - (i) Signal to noise ratio
  - (ii) Noise factor
  - (iii) Noise figure
  - (iv) Equivalent noise temperature.
- (c) Write short note on V.S.B. 6
3. (a) Explain with help of circuit diagram and waveforms high level plate modulator. 8  
(b) Compare the following amplitude modulated system : 12  
DSB-FC, DSB-SC, SSB, VSB, ISB.
4. (a) Compare A.M. with F.M. 5  
(b) Compare narrow band F.M. and wide band F.M. 5  
(c) Compare frequency modulation and phase modulation. 5  
(d) Explain F.D.M. with neat block diagram. 5
5. (a) What are the methods of F.M. generation ? Explain any one. 10  
(b) With the help of neat block diagram and waveforms explain superhetrodyne radio receiver. What are the advantages of this receiver over TRF radio receiver ? 10

4. (a) Compare A.M. with F.M. 5  
(b) Compare narrow band F.M. and wide band F.M. 5  
(c) Compare frequency modulation and phase modulation. 5  
(d) Explain F.D.M. with neat block diagram. 5
5. (a) What are the methods of F.M. generation ? Explain any one. 10  
(b) With the help of neat block diagram and waveforms explain superhetrodyne radio receiver. What are the advantages of this receiver over TRF radio receiver ? 10
6. (a) Explain phase discriminator F.M. detector with the help of circuit diagram and phaser diagram. 6  
(b) Explain PAM, PWM, PPM generation and detection. 14
7. (a) Draw the following line codes :- 5  
(i) Unipolar NRZ  
(ii) Unipolar RZ  
(iii) Polar NRZ  
(iv) Polar RZ  
(v) A.M.I. (Bipolar).
- (b) Draw the block diagram and explain PCM. 7  
(c) Draw the block diagram of Adaptive delta modulation and explain it's operation. 8  
What are the advantages of this over delta modulation ?

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Subj: **ECA&D**  
(3 Hours)

[ Total Marks : 100

(Lab)

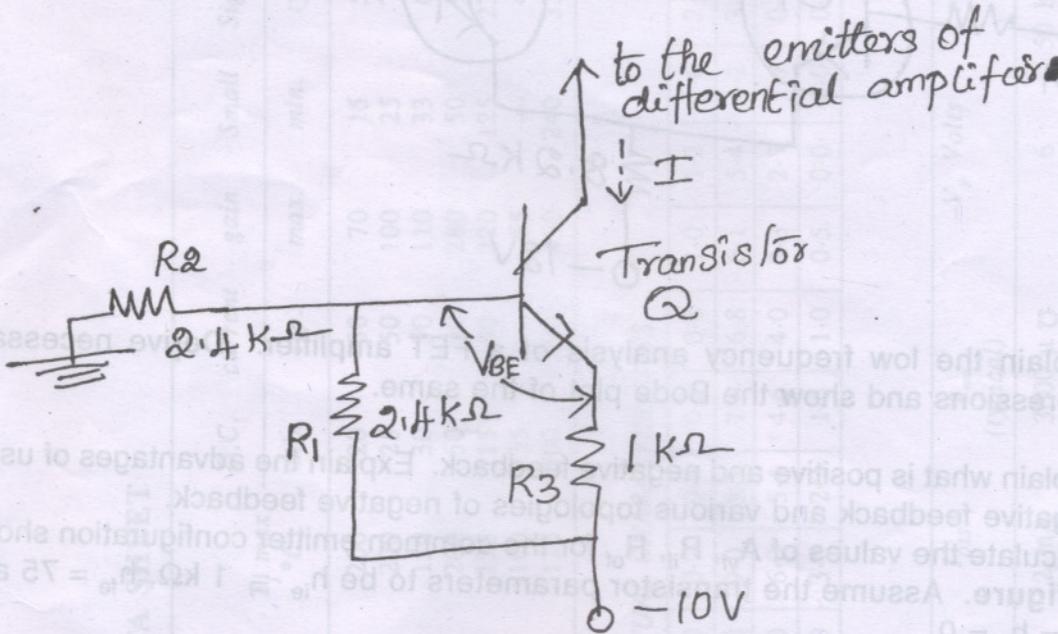
3pm to 6pm

- N.B.** (1) Question No. 1 is **compulsory**.  
 (2) Attempt any **four** questions from question Nos. 2 to 7.  
 (3) Assume **suitable** data wherever **necessary** with proper justification.  
 (4) **Figures** to the **right** indicate **full** marks.

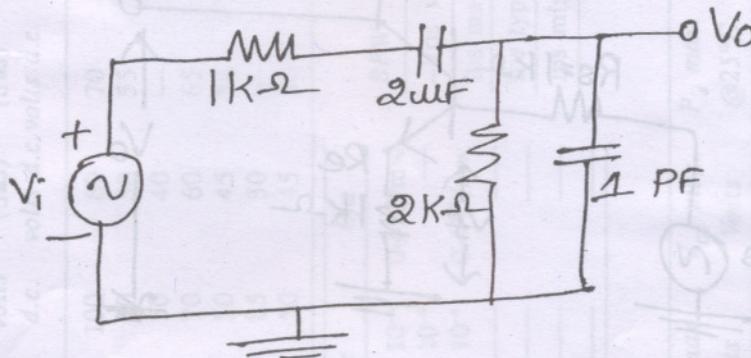
1. Attempt any **four** of the following :—

20

- (a) Draw a neat diagram and explain darlington pair. Prove that current gain of the pair is equal to the product of the individual current gains.  
 (b) Design an oscillator circuit to generate an output waveform with frequency of 2.5 MHz.  
 (c) Calculate the constant current  $I$  in the circuit shown in **figure**.



- (d) Explain what is cross-over distortion in power amplifiers. Explain how to eliminate the cross-over distortion.  
 (e) For the circuit shown in **figure** determine the corner frequencies and bandwidth of the circuit.



2. Design a two stage RC coupled amplifier for the following requirements :— 20

$$A_v \geq 1500$$

$$S_{ico} < 8$$

$$R_i \geq 1\text{m } \Omega$$

$$V_{cc} = 6\text{ volts}$$

Determine  $V_o$  max,  $R_{in}$  and  $R_o$  of the circuit.

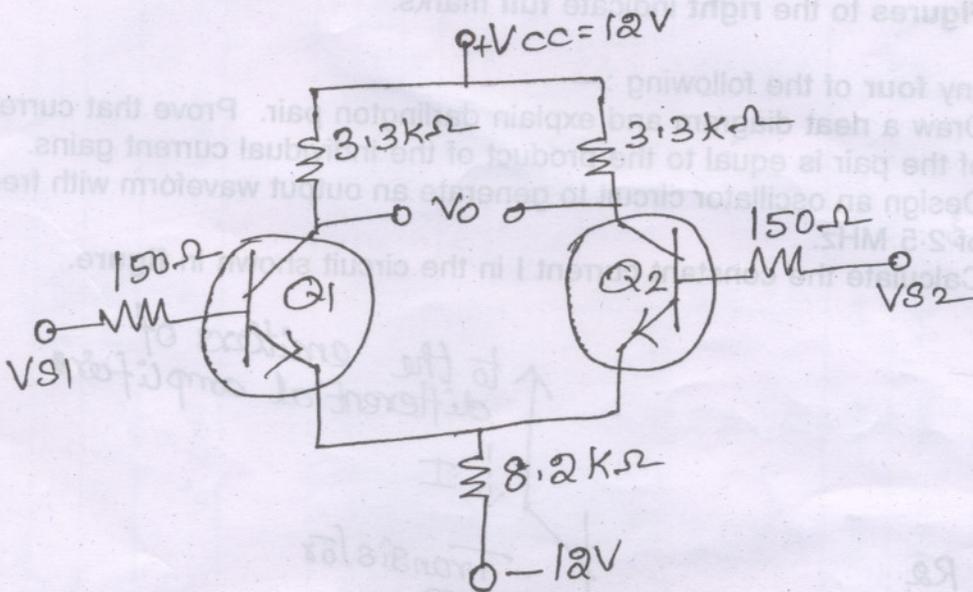
3. (a) Design class A power amplifier to provide 5 watts output to the 8 ohm load. 10
- (b) For a class B amplifier providing a  $20\text{-V}_{\text{peak}}$  signal to a  $16\ \Omega$  load (speaker) and a power supply of  $V_{cc} = 30\text{ V}$ , determine the input power, output power and circuit efficiency. 10

[ TURN OVER

4. (a) For the differential amplifier shown in **figure**, calculate :—

- (i) Operating point (ie)  $ICQ$  and  $VCEQ$
- (ii) Voltage gain ( $A_d$ )
- (iii) Input and output impedances ( $R_{in}$ ,  $R_o$ ).

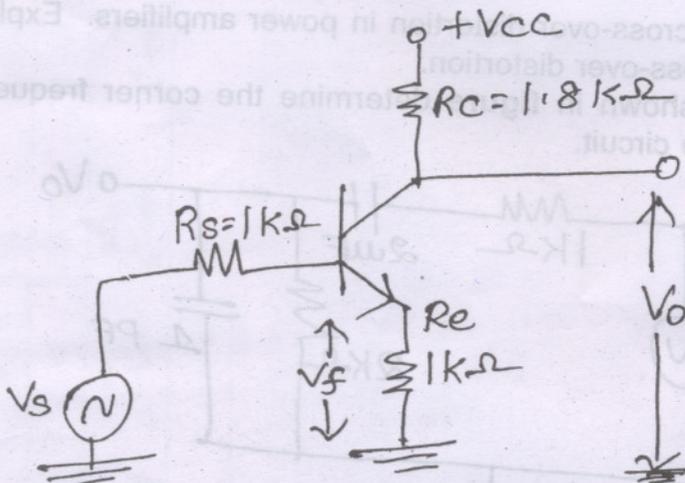
Assume  $h_{fe} = 100$  and  $h_{ie} = 1\text{ k}\Omega$ .



(b) Explain the low frequency analysis of a FET amplifier. Derive necessary 10 expressions and show the Bode plot of the same.

5. (a) Explain what is positive and negative feedback. Explain the advantages of using 10 negative feedback and various topologies of negative feedback.

(b) Calculate the values of  $A_{vf}$ ,  $R_{if}$ ,  $R_{of}$  for the common emitter configuration shown in **figure**. Assume the transistor parameters to be  $h_{ie} = 1\text{ k}\Omega$ ,  $h_{fe} = 75$  and  $h_{oe} = h_{re} = 0$ .



6. (a) Explain the requirements of multistage amplifier's. Explain the various methods of coupling multistage amplifiers with neat diagram. 10
- (b) Draw the diagram of Wien bridge oscillator and prove that the amplifier gain should be atleast equal to three (3) to ensure sustained oscillations. 10
7. Write short notes on any **three** of the following :— 20
- (a) Nyquist stability criteria to estimate stability of an amplifier.
  - (b) Cascode amplifier and applications
  - (c) Clapp oscillator
  - (d) Miller effect
  - (e) Differential amplifiers with swamping resistors.
-

## DBEC DATA SHEET

| Transistor type | $P_{dmax}$      | $I_{cmax}$     | $V_{CE}^{(sat)}$ | $V_{CBO}$     | $V_{CEO}$           | $V_{CER}$           | $V_{CEX}$     | $V_{BEO}$     | $T_j$ max | D.C. current gain |      |      | Small Signal |      | $h_{fe}$ | $V_{BE}$ max. |
|-----------------|-----------------|----------------|------------------|---------------|---------------------|---------------------|---------------|---------------|-----------|-------------------|------|------|--------------|------|----------|---------------|
|                 | @ 25°C<br>Watts | @ 25°C<br>Amps | volts<br>d.c.    | volts<br>d.c. | (SUS)<br>volts d.c. | (SUS)<br>volts d.c. | volts<br>d.c. | volts<br>d.c. |           | min               | typ. | max. | min.         | typ. |          |               |
| 2N 3055         | 115.5           | 15.0           | 1.1              | 100           | 60                  | 70                  | 90            | 7             | 200       | 20                | 50   | 70   | 15           | 50   | 120      | 1.8           |
| ECN 055         | 50.0            | 5.0            | 1.0              | 60            | 50                  | 55                  | 60            | 5             | 200       | 25                | 50   | 100  | 25           | 75   | 125      | 1.5           |
| ECN 149         | 30.0            | 4.0            | 1.0              | 50            | 40                  | —                   | —             | 8             | 150       | 30                | 50   | 110  | 33           | 60   | 115      | 1.2           |
| ECN 100         | 5.0             | 0.7            | 0.6              | 70            | 60                  | 65                  | —             | 6             | 200       | 50                | 90   | 280  | 50           | 90   | 280      | 0.9           |
| BC147A          | 0.25            | 0.1            | 0.25             | 50            | 45                  | 50                  | —             | 6             | 125       | 115               | 180  | 220  | 125          | 220  | 260      | 0.9           |
| 2N 525(PNP)     | 0.225           | 0.5            | 0.25             | 85            | 30                  | —                   | —             | —             | 100       | 35                | —    | 65   | —            | 45   | —        | —             |
| BC147B          | 0.25            | 0.1            | 0.25             | 50            | 45                  | 50                  | —             | 6             | 125       | 200               | 290  | 450  | 240          | 330  | 500      | 0.9           |

| Transistor type | $h_{ie}$       | $h_{oe}$           | $h_{re}$             | $\theta_{ja}$ |
|-----------------|----------------|--------------------|----------------------|---------------|
| BC 147A         | 2.7 K $\Omega$ | 18 $\mu \text{ S}$ | $1.5 \times 10^{-4}$ | 0.4°C/mw      |
| 2N 525 (PNP)    | 1.4 K $\Omega$ | 25 $\mu \text{ S}$ | $3.2 \times 10^{-4}$ | —             |
| BC 147B         | 4.5 K $\Omega$ | 30 $\mu \text{ S}$ | $2 \times 10^{-4}$   | 0.4°C/mw      |
| ECN 100         | 500 $\Omega$   | —                  | —                    | —             |
| ECN 149         | 250 $\Omega$   | —                  | —                    | —             |
| ECN 055         | 100 $\Omega$   | —                  | —                    | —             |
| 2N 3055         | 25 $\Omega$    | —                  | —                    | —             |

### BFW 11—JFET MUTUAL CHARACTERISTICS

| -V <sub>GS</sub> volts  | 0.0 | 0.2 | 0.4 | 0.6 | 0.8 | 1.0 | 1.2 | 1.6 | 2.0 | 2.4 | 2.5 | 3.0 |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| I <sub>DS</sub> max. mA | 10  | 9.0 | 8.3 | 7.6 | 6.8 | 6.1 | 5.4 | 4.2 | 3.1 | 2.2 | 2.0 | 1.1 |
| I <sub>DS</sub> typ. mA | 7.0 | 6.0 | 5.4 | 4.6 | 4.0 | 3.3 | 2.7 | 1.7 | 0.8 | 0.2 | 0.0 | 0.0 |
| I <sub>DS</sub> min. mA | 4.0 | 3.0 | 2.2 | 1.6 | 1.0 | 0.5 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |

### N-Channel JFET

| Type             | $V_{DS}$ max.<br>Volts | $V_{DG}$ max.<br>Volts | $V_{GS}$ max.<br>Volts | $P_d$ max.<br>@25°C | $T_j$ max. | $I_{DSS}$ | $g_{mo}$<br>(typical) | $-V_P$ Volts | $r_d$         | Derate<br>above 25°C |
|------------------|------------------------|------------------------|------------------------|---------------------|------------|-----------|-----------------------|--------------|---------------|----------------------|
| 2N3822           | 50                     | 50                     | 50                     | 300 mW              | 175°C      | 2 mA      | 3000 $\mu \text{ S}$  | 6            | 50 K $\Omega$ | 2 mW/°C              |
| BFW 11 (typical) | 30                     | 30                     | 30                     | 300 mW              | 200°C      | 7 mA      | 5600 $\mu \text{ S}$  | 2.5          | 50 K $\Omega$ | —                    |

# Con. 3336-AN-3433-10.

50 : 1st half-Exm. 10-Mina-(e)

$\theta_{jc}$   
°C/W

Derate  
above  
25°C  
W/°C

|     |      |
|-----|------|
| 1.5 | 0.7  |
| 3.5 | 0.4  |
| 4.0 | 0.3  |
| 35  | 0.05 |
| —   | —    |
| —   | —    |
| —   | —    |

|     |     |
|-----|-----|
| 3.5 | 4.0 |
| 0.5 | 0.0 |
| 0.0 | 0.0 |
| 0.0 | 0.0 |

$\theta_{ja}$

0.59°C/mW

0.59° C/mW

15 June 2010

Electronics sem IV / old

Electrical machine & Instrument

P4-Exam.-March-10-2-362

Con. 3859-10.

(OLD COURSE)

AN-3697

(3 Hours)

[Total Marks : 100

- N.B. :** (1) Q. No. 1 is **compulsory**.  
(2) Attempt any **four** questions from the remaining **six** questions.  
(3) Assume **suitable** data wherever **required**.  
(4) **Figures** to the **right** indicate **full** marks.

1. Answer any **four** :- 20
- (a) Explain the necessity of controlling torque in an indicating Instrument.
  - (b) Explain why DC series motor should never be started without mechanical load.
  - (c) Derive the balance equation of Wheatstone bridge for measurement of unknown resistance.
  - (d) Discuss why a moving Iron Instrument is suitable for both D.C. and A.C. measurements.
  - (e) The secondary winding of a current Transformers while in use should never be kept open. Why ?
2. (a) Explain different methods for the speed control of D.C. Motor. 10  
(b) A D.C. shunt motor drives a centrifugal pump whose torque varies as the square of the speed. The motor is fed from a 200 V supply and takes 50 Amp. when running at 7000 RPM. What resistance must be inserted in the armature circuit in order to reduce the speed to 800 RPM ? The armature and the field resistance of the Motor are  $0.1 \Omega$  and  $100 \Omega$  respectively. 10
3. (a) Explain in brief the various starting methods for  $3 \phi$  Induction Motor. 8  
(b) A 440 V 4 pole,  $3 \phi$  50 Hz Induction motor has motor resistance and stand still rotor reactance of  $0.025 \Omega$  and  $0.15 \Omega$  per phase. It develops a full load torque of 150 N-M at 4% slip. 12  
Determine :-  
(i) Max. torque and speed  
(ii) Value of external resistance to be inserted in each rotor phase in order to obtain Maximum torque at start.
4. (a) What do you understand by the essentials of indicating instruments ? 6  
(b) (i) Explain the construction and principle of operation electrodynamic Watt meter. 10  
(ii) State the Role of CT's and DT's in the measurements. 4
5. (a) Draw the circuit diagram of Schering bridge and derive the condition for balance. Draw the Phasor diagram. 12  
(b) Explain the working principle of a single phase Induction type energy meter, also prove that the total number of revolutions made by the disc during a particular time is proportioned to the energy consumed. 8

4. (a) What do you understand by the essentials of indicating instruments ? 6
- (b) (i) Explain the construction and principle of operation electrodynamic Watt meter. 10
- (ii) State the Role of CT's and DT's in the measurements. 4
5. (a) Draw the circuit diagram of Schering bridge and derive the condition for balance. 12  
Draw the Phasor diagram.
- (b) Explain the working principle of a single phase Induction type energy meter, also prove that the total number of revolutions made by the disc during a particular time is proportioned to the energy consumed. 8
6. (a) Explain the working and principle of a D.C. potentiometer with neat sketch and standardization. 10
- (b) Explain the construction and principle of any type of stepper motor. 10
7. Write short notes on (any **three**) :- 20
- (a) Megger with construction diagram, working principle and application
- (b) Extension of range for voltmeter and Ammeters
- (c) Starters of three phase Induction motors
- (d) Working principle of any one of the A.C. potentiometers.
-

10 June 2010

Con. 3849-10.

S.E. Electronics sem IV / old  
Principles of Microprocessor System.

(OLD COURSE)

AN-3700

(3 Hours)

[Total Marks : 100

N.B. : (1) Question No: 1 is compulsory.

(2) Attempt any four questions from remaining six.

(3) Assume suitable data if necessary and justify the same.

(4) Figures to the right indicate full marks.

- 1) a) Explain the following terms with respect to an 8085 microprocessor :- 5
- |                           |                       |
|---------------------------|-----------------------|
| i) Program counter        | iv) Instruction cycle |
| ii) Stack pointer         | v) Trap               |
| iii) Instruction register |                       |
- b) Explain the function of the following pins of 8085:- 5
- |          |                   |
|----------|-------------------|
| i) READY | iv) IO/ $\bar{M}$ |
| ii) ALE  | v) INTR           |
| iii) SOD |                   |
- c) Explain 8155 timer modes. 10
- 2) a) What are fold-back addresses? Explain with an example. 5
- b) Explain with example any five logical instructions of 8085 10
- c) Write a short note on wait state generator. 5
- 3) a) With a neat diagram explain the minimum system configuration of an 8085 microprocessor. 10
- b) Specify the contents of the registers and flags as the following instructions are executed in sequence :- 10
- ```

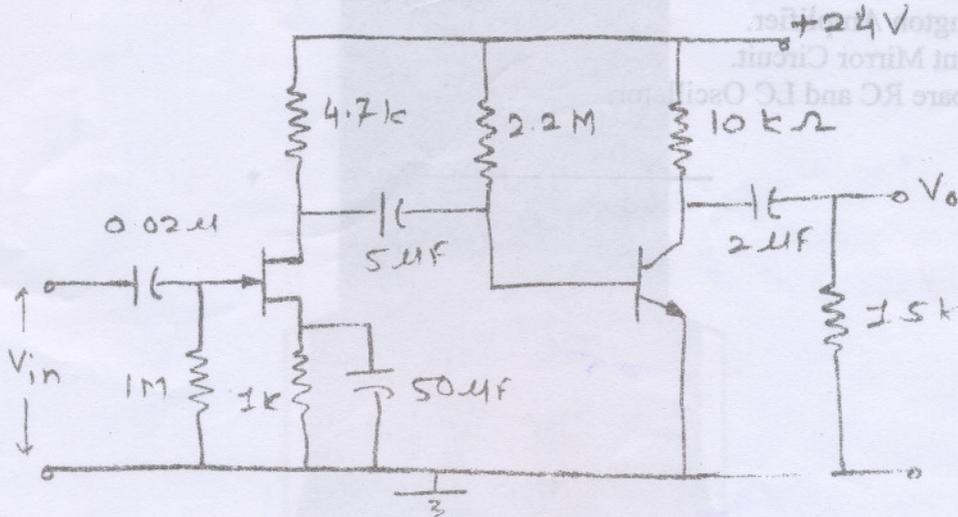
XRA A
MVI B, 4AH
MOV C, B
SUI 4FH
ANA B

```
- 4) a) What is a stack? Explain four instructions associated with a stack. 10
- b) What are reentrant and recursive subroutines? Explain various parameter-passing techniques between main program and subroutine with examples. 10
- 5) a) Explain various addressing modes of 8085 with examples 10
- b) Draw and explain interrupt structure of 8085. 10
- 6) a) Design a SBC, 8085 system using:- 12
- 4KB EPROM using 2K X 8 devices
- 8 KB RAM using 4K X8 devices
- Draw memory map and I/O map. Use exhaustive decoding. Show the generation of the various control signals
- b) Write a program to find number of ones in a given byte. Byte stored at 5000H and result at 5001H 8
- 7) a) Explain different data transfer modes of 8237 10
- b) Explain with a neat diagram, the functional organization of 8259 PIC. 10

- (Lab)
- N.B. : (1) Question No. 1 is compulsory.  
(2) Attempt any four questions from the remaining six questions.  
(3) Assume suitable data if required.  
(4) Figures to the right indicate full marks.

Q1. Design a two stage Rc Coupled amplifier for the following requirement :- (20)  
 $A_v = 1600$ ,  $S_{iCO} \leq 8$ , lower cut-off frequency  $f_L \leq 15$  Hz,  
 $V_{CC} = 9V$   
 Determine  $V_{omax}$ ,  $R_{in}$  and  $R_o$  of the circuit. (You may neglect  $h_{re}$  and  $h_{oe}$ ).

Q2. For the circuit in the figure determine the following parameters: (20)  
 (a) Dc Bias ( Q point)  
 (b) Mid frequency voltage gain( $A_v$ ) of the two stages  
 (c) Lower cutoff frequency  $f_L$  ( Separately for FET and BJT)  
 (d) Input Resistance ( $R_i$ )  
 (e) Output Resistance( $R_o$ )  
 Given : For JFET,  $I_{DSS} = 8mA$ ,  $V_p = -4V$ ,  $V_{GSQ} = -2V$   
 For BJT,  $h_{ie} = 2.5K\Omega$ ,  $\beta_{dc} = h_{fe} = 90$ ,  $V_{BE} = 0.7V$



Q3. a) Derive the expression for efficiency of transformer coupled class A Amplifier and also for class B Amplifier. (08)

b) Design a Class A power amplifier to provide 2W power to the speaker of  $4\Omega$ . (12)

Q4. a) Derive and Explain Barkhausen Criteria for Oscillation. (05)

b) Draw the circuit diagram of wein bridge oscillator. Explain its operation clearly and derive expression for frequency of oscillation. State the minimum condition to be satisfied for oscillation to take place. (10)

Con. 3338-AN-3703-10.

2

Q5. a) Explain block diagram of OP-Amp in detail. (10)

b) Using practical OP-Amp Realize : (10)

(i)  $V_o = \int V_i dt$

(ii)  $V_o = 4V_1 + V_2 - 3V_3$

Q6. a) Compare various type of negative feedback with neat diagram block. (08)

b) Analyse the dual input unbalanced output differential amplifier and obtain the expression for differential voltage gain, differential input resistance and differential output resistance. (12)

Q7. Write short notes on (Any Four) (20)

- Nyquist stability criteria.
- Heat sink.
- Darlington Amplifier.
- Current Mirror Circuit.
- Compare RC and LC Oscillator.

- N.B. : (1) Question No. 1 is compulsory.  
 (2) Attempt any four from remaining six questions.

| Q.1a) | Given are the Excitation equations and output equations in a sequential state machine. Draw the circuit diagram, write the state transition table and hence draw the state diagram<br>$D1 = F2 + X$<br>$D2 = F1, X$<br>$Z = F1, \overline{F2}$                                                                                                                                                                                                                                                                                                                                                                                                                                         | 08    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------|--------|--|-------|-------|-------|-------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Q.1b) | Write a VHDL code for an asynchronous decade counter (like 7490) using mod 5 counter and mod 2 counters as basic blocks. Use Structural architecture.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 08    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.1c) | What are different types of shift registers?                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 04    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.2a) | Design a clocked synchronous state machine for a control of tail lights of car, with three inputs as left, right and brake. There are two lights as L and R which should be blinking with left and right indicator input respectively. They both should be ON if the brake input is given. Simultaneous closure of any two inputs will indicate the error condition. Show all design steps and use minimal cost approach.                                                                                                                                                                                                                                                              | 12    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.2b) | Draw a switch debouncer using NAND gates and explain.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 08    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.3a) | Discuss two different ways in which IC 74160 can be cascaded to construct a MOD 60 counter. Explain the signal interfaces.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.3b) | Identify indistinguishable states in following state table and obtain minimized state diagram                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|       | <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">PS</th> <th colspan="2">NS</th> <th colspan="2">Output</th> </tr> <tr> <th>x = 0</th> <th>x = 1</th> <th>x = 0</th> <th>x = 1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>B</td> <td>C</td> <td>0</td> <td>0</td> </tr> <tr> <td>B</td> <td>B</td> <td>D</td> <td>0</td> <td>0</td> </tr> <tr> <td>C</td> <td>B</td> <td>C</td> <td>0</td> <td>0</td> </tr> <tr> <td>D</td> <td>E</td> <td>C</td> <td>0</td> <td>0</td> </tr> <tr> <td>E</td> <td>B</td> <td>F</td> <td>0</td> <td>1</td> </tr> <tr> <td>F</td> <td>E</td> <td>C</td> <td>0</td> <td>0</td> </tr> </tbody> </table> | PS    | NS     |       | Output |  | x = 0 | x = 1 | x = 0 | x = 1 | A | B | C | 0 | 0 | B | B | D | 0 | 0 | C | B | C | 0 | 0 | D | E | C | 0 | 0 | E | B | F | 0 | 1 | F | E | C | 0 | 0 |  |
| PS    | NS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       | Output |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|       | x = 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | x = 1 | x = 0  | x = 1 |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A     | B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C     | 0      | 0     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B     | B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | D     | 0      | 0     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| C     | B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C     | 0      | 0     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| D     | E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C     | 0      | 0     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| E     | B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | F     | 0      | 1     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| F     | E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C     | 0      | 0     |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.4a) | Design a 3 bit synchronous gray code counter using D F/F and NAND gates only.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.4b) | Using IC 74169 up /down counter and a few SSI / MSI devices design a counter which counts 0-1-2-3-4-5-6-7-6-5-4-3-2-1-0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.5a) | Write a VHDL code for the state Diagram shown. Make use of "Process" statement.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.5b) | Write short notes on (Any Two)<br>1. Metastability<br>2. Refresh operations in DRAM<br>3. Race condition and M/S JK Flip flop                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.6a) | Draw and explain logic diagram of 64 X 1 diode ROM Use two-dimensional decoding.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.6b) | With reference to XC 9500 CPLD family answer the following questions<br>1. Explain architecture of functional block<br>Which are the analog controls available in I/O block of XC9500                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.7a) | Design a serial binary Subtractor using 4:1MUX and D flip flops.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| Q.7b) | What is lockout condition? Explain with 3 bit ring counter.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 10    |        |       |        |  |       |       |       |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

# Control system of Engineering

72 : 1st half-Exm.10-Mina-(e)

Con. 3602-10.

( OLD COURSE )

AN-3694

(3 Hours)

[ Total Marks : 100

- N.B.**
- (1) Question No. 1 is **compulsory**.
  - (2) Attempt any **four** questions out of remaining **six** questions.
  - (3) **Figures** to the **right** indicate **full marks**.
  - (4) Assume **suitable** data wherever **necessary**.

1. Answer the following (any **four**) :—

20

- (a) List the types of the damping of a second order control system with location of poles.
- (b) Derive equation for peak lime of standard second order control system.
- (c) Draw step, impulse and ramp response of second order underdamped system ?
- (d) Explain how to find  $K_p$ ,  $K_v$ , and  $K_a$ .
- (e) How is gain margin and phase margin found from magnituete phase plot.

2. (a) Sketch the root locus for the system having  $G(s) H(s) = \frac{K}{s(s^2 + 2s + 2)}$  and 10

comment on stability of the system.

(b) The open loop transfer function of a unity feedback control system is given by 10

$$G(s) = \frac{k(s+5)(s+40)}{s^3(s+200)(s+1000)}$$

Discuss the stability of the closed loop system as a function of 'K', that will cause sustained oscillations in the closed loop system. What is the frequency of oscillations ?

3. (a) Draw the signal flow graph and derive the transfer function using Mason's gain 10 formula for the block diagram shown in the **figure 1** : below :—

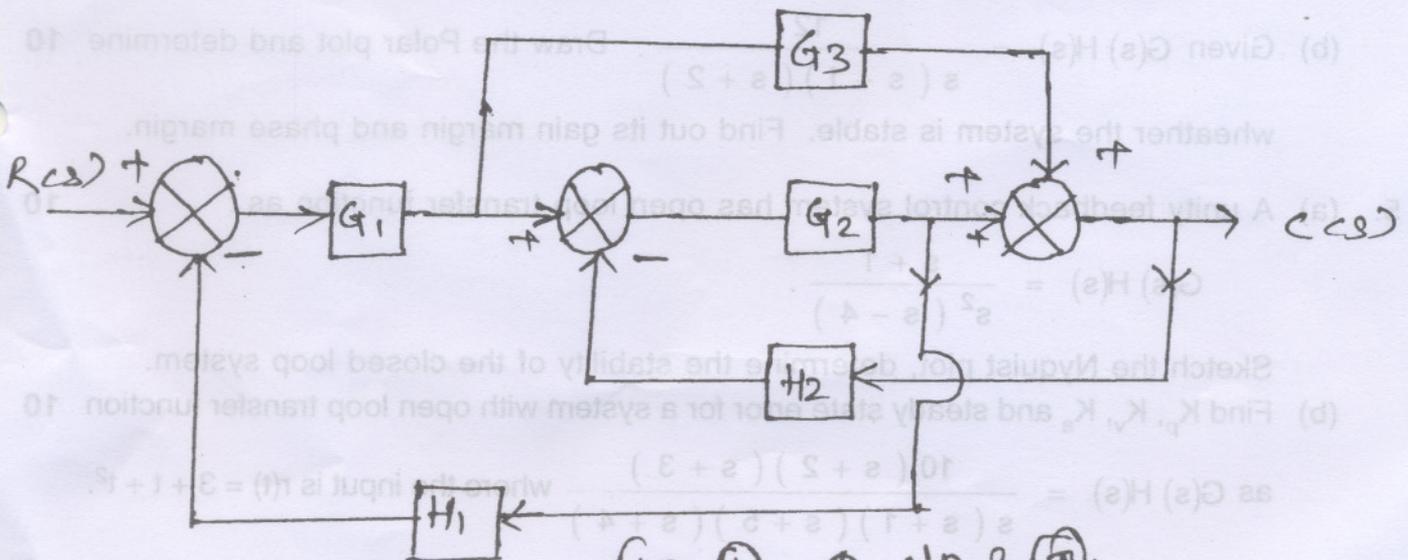


fig 1 Q. NO 3 (a)



6. (a) A second order system is given by  $\frac{C(s)}{R(s)} = \frac{2s}{s^2 + 6s + 25}$ . Find its rise time, 10

peak time, peak overshoot and settling time, if subjected to unit step input. Also calculate expression for its output response.

(b) A second order system has overshoot of 50% and period of oscillations 0.2 sec. 10  
in step response. Determine :—

- (i) Resonant peak
- (ii) Resonant frequency
- (iii) Bandwidth.

7. Write short notes on any **three** of the following :—

20

- (a) Servomechanism
- (b) PID controller
- (c) Stepper motor
- (d) M and N circles
- (e) Effect of type of system on steady state error.

2. (a) Sketch the root locus for the system having  $G(s)H(s) = \frac{K}{s(s^2 + 2s + 2)}$  and 10