			T.E. Mechanicay Electrical. Semv	
	2	Ì.	Rev / semv	
	VT-Api	ril-10- 20	, Enviormental studies.	
	Cor	n. 40	AN-4174 (REVISED COURSE)	
			(2 Hours) [Total Marks : 50	
	N.B		<ol> <li>Question No. 1 is compulsory.</li> <li>Attempt any four questions from the remaining six questions.</li> </ol>	
	1.	Atte	<ul> <li>a) Define ecology and ecosystem.</li> <li>(a) Define ecology and ecosystem.</li> <li>(b) What do you mean by Bio-energy ? Explain with example.</li> <li>(c) Explain the term "Biodiversity" with the help of an example.</li> <li>(d) How pesticides contribute to soil pollution ? Explain.</li> <li>(e) Explain the term "sustainable development".</li> <li>(f) Differenciate between exponential and geometrical population growth.</li> <li>(g) What are -3R ? Explain.</li> </ul>	0
<i></i>	<b>2</b> .	(a) (b)		5 5
	3.	(a)	Write short notes on any <b>two</b> of the following :- (i) Thermal Pollution (ii) Solid Waste Management (iii) Phopal Gas Tragedy.	5
		(b)		5
	4.	(a)	Write short notes on any <b>two</b> of the following : (i) Ecological Succession (ii) Estuaries (iii) Food Web.	5
		(b)	"It is said that next World War will be on water." Comment upon the statement giving facts.	5
	5.	(a) (b)		5 5
	6.	(a) (b)		5 5
	7.	(a)	Discuss salient features of – (i) Wild Life (Protection) Act, 1972. (ii) Forest (Conservation) Act, 1980.	5
		(b)		5
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Con. 3429-10.

T.E. Electronic & tele communication Sem V/ Rev AN-4 Microprossons & MicroControlles -(3 Hours) AN-4285 [Total Marks : 100

- **N.B.** (1) Question No. 1 is compulsory.
  - (2) Attempt any four questions from remaining six questions.
  - (3) Assume data if necessary.
- 1. (a) (i) Interface 16 KB RAM memory chip to 8085 using Absolute decoding technique. 4
  - (ii) Modify the address decoding circuit in the above design to incorporate partial decoding and thus explain the difference between Absolute decoding technique and partial decoding technique.
  - (b) (i) Draw and explain the formats of Interrupt Enable SFR and Interrupt Priority 4 SFR of 8051.
    - (ii) Write a program to enable all the interrupts of 8051 and set the priority of 4 all interrupts of 8051 to low level.
  - (c) Explain any two addressing modes of ARM processor with suitable examples. 4
- - up MOV A, C DCRC JNZ up RET
  - (i) Calculate the time delay produced by the given subroutine. Assume the **5** crystal frequency of 8085 to 6MHz.
  - (ii) Calculate the maximum time delay that can be produced by the given **5** subroutine. Assume the crystal frequency of 8085 to 6 MHz.

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- (b) Draw and explain the Internal Memory Organization of 8051.
- (a) Assume an oscillator running at 12 MHz controls 8051 micro controller. Write 10 a program to generate 2 KHz square wave on P<sub>1.0</sub> using Timer 0 in mode 1.
  - (b) Interface 8155 to 8085 in memory mapped I/O mode using Absolute decoding **10** technique.
- 4. (a) Analyze the given program and answer the following :---
  - MVIA, 4 BH
  - SIM

EI HLT

- (i) What is the status (Masked/Unmasked) of 5 Hardware interrupts of 8085 5 after executing the program and why ?
- (ii) What is the status of SOD pin after executing the program and why?
- (b) (i) Draw and explain the internal structure of port 0 of 8051.
  - (ii) Explain the features of port 3 of 8051.

5.	(a)	Interface single 8259 to 8085 in I/O mapped I/O mode using Absolute decoding technique.	10
	(b)	<ul><li>(i) Compare the Power down mode and Idle mode of 8051.</li><li>(ii) Explain any four, bit level instructions of 8051.</li></ul>	6 4
6.	(a)	<ul> <li>(i) Write a program to continuously turn ON and OFF a LED Connected to PC<sub>5</sub> of Port C of 8255 using BSR mode (8255 is connected to 8085).</li> <li>(ii) Specify the number of Machine cycles, T-states, addressing mode and number of bytes for the instruction POP PSW and INR M of 8085.</li> </ul>	6 4
	(b)	Explain the key features of ARM Processor Architecture.	10
7.	(a) (b)	Draw and explain Timing Diagram for the instruction LDAX B of 8085. Specify and explain any five instructions of ARM processor.	10 10

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(REVISED COURSE) Microprocessors & Microcontrollers I.

### (3 Hours)

[Total Marks : 100

- N.B. (1) Question No. 1 is compulsory.
  - (2) Attempt any four questions from remaining six questions.
  - (3) Assume data if necessary.
- 1. (a) (i) Interface 16 KB RAM memory chip to 8085 using Absolute decoding technique. 4
  - Modify the address decoding circuit in the above design to incorporate partial (ii) Δ decoding and thus explain the difference between Absolute decoding technique and partial decoding technique.
  - (b) (i) Draw and explain the formats of Interrupt Enable SFR and Interrupt Priority 4 SFR of 8051.
    - (ii) Write a program to enable all the interrupts of 8051 and set the priority of 4 all interrupts of 8051 to low level.
  - (c) Explain any two addressing modes of ARM processor with suitable examples. 4
- (a) Analyze the given subroutine and answer the following :----2. MVIC, O5H
  - up MOV A, C DCRC JNZ up RET
  - (i) Calculate the time delay produced by the given subroutine. Assume the 5 crystal frequency of 8085 to 6MHz.
  - (ii) Calculate the maximum time delay that can be produced by the given 5 subroutine. Assume the crystal frequency of 8085 to 6 MHz.
  - (b) Draw and explain the Internal Memory Organization of 8051.
- (a) Assume an oscillator running at 12 MHz controls 8051 micro controller. Write 3. 10 a program to generate 2 KHz square wave on P<sub>1.0</sub> using Timer 0 in mode 1.
  - (b) Interface 8155 to 8085 in memory mapped I/O mode using Absolute decoding 10 technique.
- (a) Analyze the given program and answer the following :----4.
  - MVIA, 4 BH SIM

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- (i) What is the status (Masked/Unmasked) of 5 Hardware interrupts of 8085 5 after executing the program and why ?
- (ii) What is the status of SOD pin after executing the program and why ?
- Draw and explain the internal structure of port 0 of 8051. (b) (i)
  - (ii) Explain the features of port 3 of 8051.

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Э.	(a)	i Int tec	erface single 8259 to 8085 in I/O mapped I/O mode using Absolute decoding	10
	(b)	(i) (ii)	Compare the Power down mode and Idle mode of 8051. Explain any four, bit level instructions of 8051.	6 4
6.	(a)	(i) (ii)	Write a program to continuously turn ON and OFF a LED Connected to $PC_5$ of Port C of 8255 using BSR mode (8255 is connected to 8085).	6
	(b)	Exp	Specify the number of Machine cycles, T-states, addressing mode and number of bytes for the instruction POP PSW and INR M of 8085. lain the key features of ARM Processor Architecture.	
7.	(a)	Drav	w and explain Timing Diagram for the instruction LDAX B of 8085. cify and explain any five instructions of ARM processor.	10 10 10
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Con. 3465-10.

Sub: R.f. Circuit Design AN-4279

# (REVISED COURSE)

(3 Hours)

[Total Marks : 100

### **N.B.** (1) Question No. 1 is compulsory.

- (2) Answer any four out of remaining six questions.
- (3) Assume any suitable data wherever required but justify the same.
- (4) Figures to the right indicate marks.
- 1. (a) The leads of a resistor in an RF circuit are treated as straight aluminium 6 wires ( $\sigma$  Al = 4.0 × 10<sup>7</sup>s/m) of AWG size 14 cd = 64 mil) and of total length of 5 cm.
  - (i) Compute the DC resistance
  - (ii) Find the AC resistance and inductance at 100 MHg, 1GHz, and 10 GHz operating frequencies.
  - (b) A load impedance of 40 + j 70 ohms terminates a 100 ohms transmission **6** line i.e.  $0.3 \lambda$  long. Find the reflection coefficient of the load, the reflection coefficient at the input to the line, the input impedance, the SWR in the line and the return loss.
  - (c) For the filter configuration shown in the **figure** below, the following parameters **4** are given :

 $Z_0 = 50$  ohms,  $Z_G = Z_L = Z_0$ , R = 10 ohm, L = 50 nH, C = 0.47 pF, and the generator voltage is  $V_G = 5$  V. Find the external, Internal and loaded quality factor.



- (d) Explain the design procedure of small signal BJT amplifier. (DC circuit design 4 and RF circuit design).
- (a) A particular RF circuit requires that a line impedance of 50 ohms is to be 10 maintained. A selected PCB board with dielectric constant of 4.6 and thickness of 40 mil. Find phase velocity and wavelength at 2 GHz.
  - (b) Consider the case of matching a 73  $\Omega$  load to a 50 ohm line by means of a 10  $\lambda/4$  transformer. Assume the matching is achieved for a center frequency of  $f_c = 2$  GHz. Plot the SWR for the frequency range  $1/3 \le f/f_c \le 3$ .
- 3. (a) Design a prototype low-pass Butterworth filter that will provide atleast 20 dB 10 attenuation at the frequency of  $f = 2 f_{3dB}$ . Compute and plot the amplitude response for 0 to 5 GHz.
  - (b) Plot the insertion loss of a low pass Chebyshev filter that has 6 dB ripple 10 in the passband and at least 50 dB attenuation at f = 2 f cut-off.

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 $\begin{bmatrix} s \end{bmatrix} = \begin{bmatrix} 0.15 \ 20^{\circ} & 0.85 \ -45^{\circ} \\ 0.85 \ 245^{\circ} & 0.2 \ 20^{\circ} \end{bmatrix}$ 

Determine whether the transistorized Network is Reciprocal and lossless. If port 2 is terminated with a matched load, what is the return loss seen at port 1? If port 2 is terminated with a short circuit, what is the return loss seen at port 1?.

- (b) A BJT is encapsulated in a plastic housing and mounted on a heat sink 10  $(R_{thha} = 3.75 \text{ °C/w})$  under these conditions the total power dissipation is supposed to be 20 w. at an ambient temperature of 20 °C. What rating has the engineer to choose for the BJT casing if the maximum junction temperature should not exceed 175 °C.
- 5. (a) For small signal BJT amplifier shown, find the value of inductor that would provide negative feedback above f = 600 MHz. Assume that the phase of  $S_{21}$  approaches 90° around 600 MHz.



- (b) An abrupt pn-junction made of S<sub>i</sub> has the acceptor and donor concentrations 12 of N<sub>A</sub> =  $10^{18}$  cm<sup>-3</sup> and N<sub>D</sub> =  $5 \times 10^{15}$  cm<sup>-3</sup>, respectively. Assuming that the device operates at room temperature, determine :
  - (i) The barrier voltage
  - (ii) The space charge width in the p and n type semiconductors.
  - (iii) The peak electric field across the junction.
  - (iv) The junction capacitance for a cross sectional area of  $10^{-4}$  cm<sup>2</sup> and a relative dielectric constant of  $\epsilon_r = 11.7$ .
- (a) For the simplified FET model shown determine the capacitances C<sub>gs</sub> and C<sub>gd</sub> 10 as well as g<sub>m</sub>. Show that for low frequency operation it is sufficient to record the drain current and gate-source voltage under short circuit output condition.



- (b) Plot and compare the frequency response of BJT, FET and HEMT.
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- 7. Write short notes on following :---
  - (a) Chip components
  - (b) Matching Networks
  - (c) Parallel and series connections
  - (d) Coupled Filters.

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Con. 3465-10.

AN-4279

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## (REVISED COURSE)

R.F. circuit Design.

T.E. ETRCS & tele communication

(3 Hours)

[ Total Marks : 100

### N.B. (1) Question No. 1 is compulsory.

- (2) Answer any four out of remaining six questions.
- (3) Assume any suitable data wherever required but justify the same.
- (4) Figures to the right indicate marks.
- 1. (a) The leads of a resistor in an RF circuit are treated as straight aluminium wires ( $\sigma$  Al = 4.0 × 10<sup>7</sup>s/m) of AWG size 14 cd = 64 mil) and of total length of 5 cm.
  - (i) Compute the DC resistance
  - (ii) Find the AC resistance and inductance at 100 MHg, 1GHz, and 10 GHz operating frequencies.
  - (b) A load impedance of 40 + j 70 ohms terminates a 100 ohms transmission line i.e. 0.3  $\lambda$  long. Find the reflection coefficient of the load, the reflection coefficient at the input to the line, the input impedance, the SWR in the line and the return loss.
  - (c) For the filter configuration shown in the **figure** below, the following parameters are given :

 $Z_0 = 50$  ohms,  $Z_G = Z_L = Z_0$ , R = 10 ohm, L = 50 nH, C = 0.47 pF, and the generator voltage is  $V_G = 5$  V. Find the external, Internal and loaded quality factor.



- (d) Explain the design procedure of small signal BJT amplifier. (DC circuit design 4 and RF circuit design).
- (a) A particular RF circuit requires that a line impedance of 50 ohms is to be 10 maintained. A selected PCB board with dielectric constant of 4-6 and thickness of 40 mil. Find phase velocity and wavelength at 2 GHz.
  - (b) Consider the case of matching a 73  $\Omega$  load to a 50 ohm line by means of a 10  $\lambda/4$  transformer. Assume the matching is achieved for a center frequency of  $f_c = 2$  GHz. Plot the SWR for the frequency range  $1/3 \le f/f_c \le 3$ .
- 3. (a) Design a prototype low-pass Butterworth filter that will provide atleast 20 dB 10 attenuation at the frequency of  $f = 2 f_{3dB}$ . Compute and plot the amplitude response for 0 to 5 GHz.
  - (b) Plot the insertion loss of a low pass Chebyshev filter that has 6 dB ripple 10 in the passband and at least 50 dB attenuation at f = 2 f cut-off.

**[ TURN OVER** 

4. (a) A two-port transistorized Network have the following scattering matrix :

$$[s] = \begin{bmatrix} 0.15 & 0^{\circ} & 0.85 & -45^{\circ} \\ 0.85 & 45^{\circ} & 0.2 & 0^{\circ} \end{bmatrix}$$

Determine whether the transistorized Network is Reciprocal and lossless. If port 2 is terminated with a matched load, what is the return loss seen at port 1? If port 2 is terminated with a short circuit, what is the return loss seen at port 1?.

- (b) A BJT is encapsulated in a plastic housing and mounted on a heat sink 10  $(R_{thha} = 3.75 \text{ °C/w})$  under these conditions the total power dissipation is supposed to be 20 w. at an ambient temperature of 20 °C. What rating has the engineer to choose for the BJT casing if the maximum junction temperature should not exceed 175 °C.
- 5. (a) For small signal BJT amplifier shown, find the value of inductor that would **8** provide negative feedback above f = 600 MHz. Assume that the phase of  $S_{21}$  approaches 90° around 600 MHz.



- (b) An abrupt pn-junction made of S<sub>i</sub> has the acceptor and donor concentrations 12 of  $N_A = 10^{18}$  cm<sup>-3</sup> and  $N_D = 5 \times 10^{15}$  cm<sup>-3</sup>, respectively. Assuming that the device operates at room temperature, determine :
  - (i) The barrier voltage
  - (ii) The space charge width in the p and n type semiconductors.
  - (iii) The peak electric field across the junction.
  - (iv) The junction capacitance for a cross sectional area of  $10^{-4}$  cm<sup>2</sup> and a relative dielectric constant of  $\epsilon_r = 11.7$ .
- 6. (a) For the simplified FET model shown determine the capacitances  $C_{gs}$  and  $C_{gd}$  10 as well as  $g_m$ . Show that for low frequency operation it is sufficient to record the drain current and gate-source voltage under short circuit output condition.



(b) Plot and compare the frequency response of BJT, FET and HEMT.

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- 7. Write short notes on following :---
  - (a) Chip components
  - (b) Matching Networks
  - (c) Parallel and series connections
  - (d) Coupled Filters.

T.E. Electronics & felc com cartion sem V. Rev. Principle of control systems (REVISED COURSE)

[Total Marks : 100

- N.B. (1) Question No. 1 is compulsory.
  - (2) Answer any four out of remanining six questions.
  - (3) Figures to the right indicate full marks.
  - (4) Illustrate answers with sketches wherever required.
- (a) Define sensitivity. How can we reduce the sensitivity of closed loop system? 20 1.
  - (b) State the properties of Transfer function.
  - (c) Explain Hurwitz Stability Criterion. What are the Disadvantages ?
  - (d) What are the advantages of Bode Plot ?

(a) Determine the value of  $V_{a}(t)$  if — 2.



termine the value of	$\mathbf{v}_{0}(\mathbf{r}) \cdots \cdots \cdots$		
$C_2 = 5C_1$	, ,		
$V_{1}(t) = 40 \cdot e^{-20t}$	CI		
$C_1 = 0.5 \text{ uf}$			
$R = 100 m\Omega$			-0
			1'
	VII-0 K		$V_{n}(t)$
	~ -0		× U =
	() Vi(+)		}
		l	VI.

- (b) Explain the effect of an additional zero and additional pole to the standard second 10 order system.
- (a) Consider the following block diagram shown in figure below. Draw its equivalent 10 3. signal flow graph and find C(s)/R(s) using Mason's gain formula.



(b) Derive the transfer function of armature controlled dc servomotor and obtain the 10 resulting block diagram.

**[TURN OVER** 

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Con. 4025-10.

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### Con. 4025-AN-4282-10.

 (a) Using block diagram reduction rule, obtain the transfer function of the system shown 10 in figure below :—

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(b) The open loop transfer function of a feedback system is ---

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$$G(s) H(s) = \frac{K}{s(s+4)(s^2+4s+20)}.$$

Draw complete root locus. Determine value of K for stability. Determine oscillation frequencies.

5. (a) Determine the value of K for unity feedback control system having -

G(s) H(s) = 
$$\frac{K}{s(s+2)(s+4)}$$

- (i) Phase margin =  $60^{\circ}$
- (ii) Gain margin = 20 dB
- (b) Derive and analyse the response of a second order system to a unit step. With the **10** help of graphical plots explain the significance of damping ratio for its various values.

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### 6. (a) The output of a control system is related to its input by --- 12 $(s^4 + 2s^3 + 2s^2 + (3 - K) s + K) C(s) = K(s + 1) R(s)$

Where K represents the positive gain of an amplifier.

- (i) With K = 6 and a step input will the output response be stable ?
- (ii) Determine the limiting value that K can have for a stable output response.
- (b) Obtain the Transfer function of field controlled D.C. Motor. Draw block diagram. 8
- 7. Write short notes on any two of the following :---
  - (a) A. C. Servomotors
  - (b) Tachogenerators
  - (c) Error compensation methods and their effects on system performance.

TFC: Electromics & telecomunication Date  
Exam / Random signal Analysis 28 may zoto  
Con. 3436-10. (REVISED COURSE) AN-4276  
Sem TC (3 Hours) 
$$R_{eVic}$$
 [Total Marks : 100  
N.B. (1) Question No. 1 is computery.  
(2) Attempt any four questions from the remaining questions.  
(3) Assume any suitable data if necessary.  
(a) Assume any suitable data if necessary.  
(b) Apriori or Classical definition.  
(c) Apriori or relative frequency definition.  
(c) Apriori or relative trequency definition.  
(c) Apriori or relative trequency definition.  
(c) Apriori or relative trequency definition.  
(c) State and prove Bay's theorem.  
(c) State and prove Bay's theorem.  
(c) State and explain joint and conditional probabilities of events.  
(d) State and explain joint and conditional probabilities of events.  
(e) State and explain joint and conditional probabilities of events.  
(f) State and explain joint and conditional probabilities of events.  
(g) State and explain joint and conditional probabilities of events.  
(g) State and explain joint and conditional probabilities of events.  
(g) State and respin (priori and conditional probabilities of events.  
(g) State and respin (priori and conditional probabilities of events.  
(g) State and respin (priori and conditional probabilities of events.  
(g) Find the value of normalization constant C.  
(ii) f(x)  
(iii) F<sub>x</sub>(y)  
(iv) F<sub>x</sub>(xy)  
(iv) F<sub>x</sub>(xy)  
(iv) E(y/x)  
(iv) E(y/x)  
(iv) E(y/x)  
(iv) Mechanism consist of three paths A, B, C and probabilities of their failure  
are p.q. respectively. The mechanism work if there is no failure in any of  
these parts. Find the probability that-  
(i) Mechanism is working  
(ii) Acontinuous random variable has the probability density function.  
f(x) = 6(x - x') & 0 \le x \le 1  
Find mean and variance.  
[TURN OVER]

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### Con. 3436-AN-4276-10.

4. (a) State and prove properties of autocorrelation function and cross correlation 10 function.

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(b) The power spectrum of WSS process x(t) is given by

$$S(w) = \frac{1}{\left(\cdot 1 + \omega^2\right)^2}$$

Find its auto correlatin functin  $R(\tau)$  and average power.

- 5. (a) A random process is defined by  $X(t) = A \cos (\omega_0 t + \theta)$  where A and  $\omega_0$  are **10** constants and  $\theta$  is random variable uniformly distributed over (0,  $2\pi$ ). Show that process is erotic in mean and also in corelation.
  - (b) Find the power spectral density function of random process whose autocorrelation **10** function is—

$$R(\tau) = 1 - (|\tau|/T) , |\tau| \le T$$
$$= 0 , elsewhere$$

- 6. (a) (i) Define central limit theorem and give its significance.
  - (ii) Define strong law of large numbers.
  - (iii) Describe sequence of random variables.
  - (b) (i) If today is Wedensday and whether is in state 2 what is the probability that the whether is in state 3 on Thursday and the state 1 on Friday ?
    - (ii) What is the probability whether on Friday is in state 1, given that it is in state 2 on Wednesday ?
- 7. (a) Consider that the society is divided into three income grows, low, middle and **10** high, suppose that the transition probability that the next generation will grow from one income group to the other or will be in the same group is as given below :

L		M	н
L	0.45	0.48	0.07
Μ	0 45 0 05 0 01	0.7	0.25
Н	0.01	0.5	0.49

Find the limiting probabilities.

(b) Find the characteristic function of the Laplace distribution.

 $f(x) = (m/2) e^{-mixi}, -\infty < x < \infty.$ 

Also find its mean and variance.

8 : 1st half.10-AM(I) Con. 3724-10.

# T.F. Electronics & relecommunication Sem V/fer (REVISED COURSE) Signers & Systems. (3 Hours)

[Total Marks: 100

- N.B.: (1) Question No. 1 is compulsory.
  - (2) Attempt five questions in all.
  - (3) All parts of the same questions must be written in continuation.
  - (4) Assume suitable data, if required and state them clearly.
- Answer any four of the following :---1.
  - (a) Find the ROC of the given signal  $x(t) = 3e^{-2t} u(t) - 2e^{-t} u(t).$
  - (b) Determine the direct form I realisation for the following transfer function  $H(z) = 1 - 0.7 z^{-1} + 0.4 z^{-2}$
  - (c) A linear-time invariant (LTI) system is characterized by the following difference equation :

y(n) = a y(n - 1) + b x(n) for 0 < a < 1

Find the magnitude and phase of the frequency response H(e<sup>jw</sup>) of the system.

(d) Determine the signal energy and signal power for the following signals :

(i) 
$$x(t) = e^{-3Ut}$$

(ii)  $x(t) = e^{-3t}$ 

(e) State and explain convolution property of Z-transform.

- (a) Consider the analog signal  $x_a(t) = 5 \sin 200\pi t$ 2.
  - Determine the minimum required sampling rate to avoid sampling. (i)
  - (ii) Suppose that the signal is sampled at the rate  $F_s = 100$  Hz. What is the discrete time signal obtained after sampling ?
  - (iii) Suppose that the signal is sampled at the rate  $F_s = 300$  Hz, what is the discrete time signal obtained after sampling .
  - Impulse response of a discrete-time LTI system is expressed as under : 10 (b)  $h(n) = \{1, 2, 3\}$ Find the i/p sequence x(n) for output response which is given by ---

 $y(n) = \{ 1, 1, 2, -1, 3 \}.$ 

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3. (a) Compute the response of the system y(n) = 0.7 y(n-1) - 0.12 y(n-2) + x(n-1) + x(n-2) 10 to input x(n) = nu(n). Is the system stable ?

- (b) Obtain the Fourier transform of a rectangular pulse of duration 2 seconds and **10** having a magnitude of 10 volts.
- 4. (a) Find the Fourier series for the function x(t) defined by

$$\mathbf{x}(t) = \begin{cases} 0 & \frac{-T}{2} < t < 0 \\ A \sin w_0 t & 0 < t < \frac{T}{2} \end{cases}$$

and 
$$x(t + T) = x(t)$$
,  $W_0 = \frac{2\pi}{T}$ .

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oid Exam/ Elements of Microelectronics.

VT-April-10- 203

Con. 3996–10.

### (OLD COURSE)

AN-4063

(3 Hours)

### [ Total Marks:100

- **N.B.**: (1) Question No. 1 is compulsory.
  - (2) Attempt any four from the remaining questions.
  - (3) Assume suitable data wherever necessary.
- (a) With the help of a neat diagram explain the important features of butting 5 and buried contact.
   (b) What buried layer ? What is its importance in BJT technology. 5
  - (c) What are the different ways to adjust threshold voltage of MOSFET.
  - (d) What are the advantages of twin-tube process over n-well process.
- 2. (a) Explain with neat diagram fabrication of CMOS Inverter using n-well **10** technology.
  - (b) Discuss parasitic effects in MOSFET.
- 3. (a) What are the different types of MOSFET scaling ? Explain each in detail **10** with their advantages and disadvantages.
  - (b) What are short channel effects ? Explain in detail.
- 4. (a) Draw the layout of 2 input CMOS NAND gate using λ (lambda) rules. 10
  (b) Draw transfer characteristics of CMOS Inverter and explain it in detail. 10
- 5. (a) Calculate the threshold voltage  $V_{TO}$  at  $V_{SB} = 0$ , for a polysilicon gate 10 n-channel MOSFET with the following parameters :--
  - (i) Substrate doping density  $N_A = 10^{16} \text{ cm}^{-3}$
  - (ii) Polysilicon gate density  $N_p = 2 \times 10^{20} \text{ cm}^{-3}$
  - (iii) Gate oxide thickness tox = 500 A°
  - (iv) Oxide-interface charge density Nox =  $4 \times 10^{10}$  cm<sup>-2</sup>.

Data :  $\left(\frac{KT}{q}\right) = 26 \text{ mV}, \text{ ni} = 1.45 \times 10^{10} \text{ cm}^{-3}, \text{ q} = 1.6 \times 10^{-19} \text{ Col},$   $\epsilon_{o} = 8.85 \times 10^{-14} \text{ F/cm}, \epsilon_{si} = 11.7 \times \epsilon_{o} \text{ F/cm},$  $\epsilon_{ox} = 3.97 \times \epsilon_{o} \text{ F/cm}.$ 

(b) Explain in detail ion implantation technique.

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- 6. (a) What are different techniques used to grow single crystal silicon? Explain 10 any one in detail.
  - (b) Implement following function using standard CMOS. Also draw stick diagram. 10

(i) 
$$Z = (A + B)$$
 (C + D) + AD  
(ii)  $Z = \overline{\overline{A} \overline{B} + AB}$ 

- 7. Write short notes on any four :-
  - (a) Photolithography
  - (b) CMOS Latchup
  - (c)  $\lambda$ -based Layout Rules
  - (d) TTL NAND Gate
  - (e) IC Cross Overs.

T.E. Electronic & tele communication 28 May 2010 (JEM V) old Exam P4--Exam --March--10--2--26 (OLD COURSE) AN-4054 Con. 3398-10. [Total Marks : 100 (3 Hours) N.B.: (1) Attempt any five guestions. (2) Assume suitable data if necessary. (3) Figures to the right indicate full marks. 20 Write short notes (any two) :-1. (a) Difference between active and passive differs (b) Switched capacitor Akerberg Mossberg filter (c) Properties of a Butterworth function. 10 Derive the Transfer function of Sallen and Key low-pass filter. 2. (a) 10 Synthesize a passive network to realize the transfer function given below with  $1\Omega$ (b) termination resistor :-- $Y_{T}(s) = \frac{s(s^{2} + 9)}{2s^{3} + s^{2} + 8s + 1}$ Determine the Transfer function of the following circuit :-10 (a) З. 2F-IF Develop and implement a second order normalized low pass Butterworth filter 10 (b) transform it to a normalized Band reject filter. Sketch the gain versus frequency for the voltage transfer function given below:- 10 4. (a)  $T(s) = 10 \frac{s^2 + 16}{s^2 + 2s + 100}$ Draw the circuit configuration for Generalized Impedance Converter (GIC). Analyse 10 (b) it and determine transmission parameters.

5. (a) What is bi-quadratic function, identify the bi-quadratic parameters K,  $W_2$ ,  $W_P$ ,  $Q_2$ ,  $Q_P$  10

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from the following function 
$$H(s) = \frac{4s^2 + 16}{2s^2 + 6s + 12}$$
.

(b) Synthesize the following function :-

$$Z(s) = \frac{s^3 + 2s}{s^2 + 1}$$

6. (a) Explain how resistor is realized by a MOS switched capacitor.
(b) Synthesize the following function -

$$Z(s) = \frac{s(s^2 + 2)}{(s^2 + 1)(s^2 + 3)}$$

7. (a) Find the denormalized network for the given network circuit and Transfer function 10

$$N_n(p) = \frac{0.6p}{p^2 + 0.6p + 2}$$
 and cut-off frequency  $f_c = 10$  KHz.

(b) Draw the neat circuit diagram of Tow-Thomas filter and derive the transfer function **10** for low pass and band pass filter realizations.

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		,		£1.	ements	0 F	Micro	oprocess	sors.	2 J	une 201
	Con. 3	3402-10.		(		SE)		A	N-4066		. Sec.
					(3 Hours	s)		[ Total Mar	'ks:100		
	<b>N.B.</b> (	1) Question	No. 1 is	compuls	sory.						
	(2	2) Attempt	any <b>four</b>	out of re	maining six	ζ.					
	(\$	3) Assume	suitable	data whe	erever <b>nece</b>	ssary.					
()	1. De	esign 8086 b	ased micr	oprocess	or system w	ith follow	/ina specif	ications –		20	
		(a) CPU v			•		0 - 1				
- 1		(b) Nume	ric data pr	ocessor,	8087						
		(c) 32 kB	SRAM us	ing 8 kB o	devices						
		(d) 64 kB	EPROM u	ising 16 k	B devices						
		(e) Two, 8	3 bit input	parts							• •
$\sim$		(f) Two, 8	3 bit outpu	t parts.							
		Show men	nory map	and I/o m	ap with deco	oding log	ic. Use al	osolute deco	oding.		
	2. (a)	) Write an a	ssembly la	inguage j	program for	8085 to f	find positiv	ve, negative	numbers	10	
		in an array						-			
	(b)	) Write an a 'MICROPF			program usi	ng 8086	instructio	ns to display	y a string	10	
	3. (a)	Explain ser used for th		nication w	ith 8085 micr	oprocess	sor. Also m	ention the ins	structions	10	
	(b)	Draw and e		ing diagr	am for STA	2050 h.				10	
- -	4 (a)	Explain IC\	Ns and O	CWs at 8	250 PIC					40	
		Draw the fu				and evr	alain its m	ndes at oner	ation	10	
•				noon ulay				איר איר איראיראיראיראיראיראיראיראיראיראיראיראירא	auon.	10	
$\bigcirc$	5. (a)	Explain the	interrupts	of 8086	microproces	sor.				10	
	(b)	Explain all	the addre	ssing moo	des of 8086	with exa	mples.			10	
	6. (a)	What do yo	ou mean b	y mixed la	anguage pro	grammir	ng ? Expla	ain with an e	example	10	
		containing	IF-THEN-	ELSE sta	tement.						
	(b)	Explain the	role of 82	88 bus c	ontroller in n	naximum	i made of a	8086.		10	
	7. Wri	ite short note	es :-							20	
		(a) Modes	of DMA tr	ansfer							
		(b) Assem	bler direct	ives							
		(c) 8254 P	PIT.								

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Con. 3642–10.

# (OLD COURSE) Computer Architecture & Organisettion (3 Hours) [Total Marks: 100

- **N.B.** :(1) Question No. 1 is compulsory.
  - (2) Attempt any four questions out of remaining six questions.
- 1. (a) Distinguish Hardwired and Microprogrammed control unit. 7 (b) Explain stops involved in design of ALU. 7 (c) Differentiate between RISC and CISC characteristics. 6 2. (a) Explain the control unit design for gcd processors using state table method. 10 (b) Explain the different mapping techniques used in the design of Cache 10 memory. 3. (a) Write a short note on MIMD. 10 (b) Explain the use of Guard bits and Rounding methods for floating point 10 numbers. (a) Explain any two hardwired control unit design techniques. 4. 10 (b) Explain any two techniques of bus arbitration. 10 (a) Distinguish interrupt driven I/O and programmed I/O. 5. 10
  - (b) Explain Booth's algorithm for multiplication of signed numbers. **10**
  - 6. (a) What do you mean by addressing mode? Explain addressing modes. 10
    (b) Write the necessity of page replacement algorithm? List and explain 10 different page replacement algorithms.
  - 7. (a) Compare SRAM and DRAM.
    - (b) What are advantages of pipelining ? Explain with respect to a floating 12 point data path. Prove that for a K stage pipeline, the speed up factor = K.

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Con. 3642–10.

# Sub: C.A & O (OLD COURSE)

AN-4057

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(3 Hours)

- [ Total Marks : 100
- N.B. :(1) Question No. 1 is compulsory.
  (2) Attempt any four questions out of remaining six questions.
- 1. (a) Distinguish Hardwired and Microprogrammed control unit.
  - (b) Explain stops involved in design of ALU.
    - (c) Differentiate between RISC and CISC characteristics.
- 2. (a) Explain the control unit design for gcd processors using state table method. 10
  - (b) Explain the different mapping techniques used in the design of Cache **10** memory.
- 3. (a) Write a short note on MIMD.
  - (b) Explain the use of Guard bits and Rounding methods for floating point **10** numbers.
- 4. (a) Explain any two hardwired control unit design techniques.
  (b) Explain any two techniques of bus arbitration.
  10
- 5. (a) Distinguish interrupt driven I/O and programmed I/O.10(b) Explain Booth's algorithm for multiplication of signed numbers.10
- 6. (a) What do you mean by addressing mode? Explain addressing modes. 10
  (b) Write the necessity of page replacement algorithm? List and explain 10 different page replacement algorithms.
- 7. (a) Compare SRAM and DRAM.
  - (b) What are advantages of pipelining ? Explain with respect to a floating 12 point data path. Prove that for a K stage pipeline, the speed up factor = K.

T.E. Electronics & Fere Sem VI 010. Ommunicention Circuits.

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### Con. 3793-10.

## (OLD COURSE)

## AN-4060

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(3 Hours)

[ Total Marks : 100

- N.B. (1) Question No. 1 is compulsory.
  - (2) Attempt any four questions out of remaining six questions.
  - (3) Draw suitable diagrams wherever needed.
  - (4) Make suitable assumption wherever need and mention the same.
  - 1. Answer the following questions any four :-
    - (a) Describe LM 380 as phono-amplifier
    - (b) With neat sketch explain first order digital phase locked loop
    - (c) Explain about capture range and lock range in PLL. Which one is greater ? Why ?
    - (d) Discuss input compensation technique for broadbanding
    - (e) What is meant by hybrid tranformer ?
  - 2. (a) Design a Direct Digital Frequency Synthesizer to generate  $15.8 \times 10^6$  Hz from a 10  $1 \times 10^6$  Hz reference oscillator.
    - (b) Discuss in detail the analysis of a series RLC circuit with pole-zero diagram. 10
  - 3. (a) Derive the equation for noise factor of a cascaded five networks. 10
    - (b) What minimum input signal will give output signal to noise ratio of 0 db in a system **10** with input impedance of 50  $\Omega$ , a noise figure of 8 db and a bandwidth of 2.1 KHz ? Take operating temperature as 290 K.
  - 4: (a) Derive transfer function of second order PLL and explain magnitude plot as function **10** of frequency for this PLL.
    - (b) Explain frequency synthesizer that uses variable modulus divider.
    - (c) Explain how switching time can be reduced in frequency synthesizer.
  - 5. (a) Explan how impedance level shifting can be accomplished in narrow band circuits **10** without incurring cost of expensive and bulky transformer. Include proper mathematics for justification.
    - (b) Explain different methods of neutralization and feedback technique used in wideband **10** amplifiers.
  - 6. (a) Design a loss less coupling network that match a load of  $(12 + j5) \Omega$  to a 40  $\Omega$  10 source impedance of 20 MHz.
    - (b) Explain use of PLL as :-
      - (i) Traking filter
      - (ii) Signal synchronizer.
  - 7. Write short notes any two :-
    - (a) Switching type mixer
    - (b) AM modulator using 1596
    - (c) Parallel RLC circuit giving an application
    - (d) Hybrid transformer.