8/6/2022

1sthalf-11-SG 84-(C)

B.E. E&TC VII (Rev) Communication Networks

Con.3852-11 **(REVISED COURSE)** **RK-3345**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Illustrate** answers with sketches wherever **required**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Explain LAN Topologies with neat diagram. 20
(b) Write a note on flow control in data link layer.
(c) Explain congestion control in Datagram Subnet.
(d) Explain TCP/IP utilites.

2. (a) Explain various transmission media in detail. 10
(b) What is role of Modem ? Explain XDSL in detail. 10

3. (a) Explain SONET/SDH in detail. 10
(b) Explain stop and wait ARQ, Go-back-N ARQ, Selective repeat ARQ. 10

4. (a) What is HDLC Protocol ? What are three frame types supported by HDLC ? Describe each in detail. 10
(b) Explain static and dynamic routing algorithms. 10

5. (a) With the help of neat diagram explain packet switching and virtual circuit packet switching and also explain their advantages and disadvantages. 10
(b) Explain in detail Repeater, Hub, Bridges, Routers, Gateway, Switches. 10

6. (a) Write a note on IEEE 802-3 Standard in detail. 10
(b) Explain Berkeley Application Programming Interface in detail. 10

7. (a) Explain Terminal Network (TELNET) and File Transfer Protocol (FTP). 10
(b) Draw the layered OSI network architecture. Explain the function of each layer in detail. 10

BE ETRX VII (REV)
Elective II Digital Image Processing Design.

17. 1st Half-Exam.-11 mina-(d).

Con. 3994-11. **(REVISED COURSE)** **RK-3342**

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** out of remaining **six** questions.
(3) **Figures** to the **right** indicates **full** marks.
(4) Assume **suitable** data if **necessary**.

1. Justify/Contradict following statements :— 20
   (a) All image compression techniques are invertible.
   (b) Quality of picture depends on the number of pixels and gray level that represent the image.
   (c) The first difference of chain code normalize it to rotation.
   (d) Walsh Transform matrix is nothing but sequency ordered Hadamard matrix.

2. (a) A 64 x 64 image, represented by 3 bit/pixel has the following grey level distribution :— 10

Gray level	0	1	2	3	4	5	6	7
No. of Pixel	128	75	280	416	635	1058	820	684

   Perform Histogram Equalization and give new distribution of gray level. Show plots of original and equalized image.

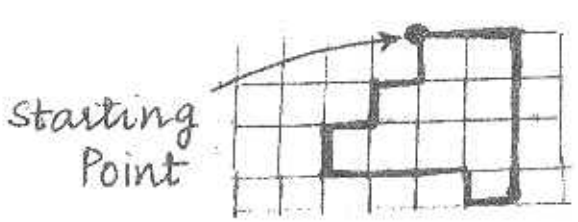
   (b) Prove that if an image f(m, n), $0 \leq m \leq M-1$ and $0 \leq n \leq N-1$ is multiplied by the checkerboard pattern $(-1)^{m+n}$, then its DFT is centered at $\left(\frac{M}{2}, \frac{N}{2}\right)$. 10

3. (a) Assuming that the edge starts on the first column and ends in the last column for the following gray level image :— 10

   2 1 0
   1 1 7
   6 8 2

   Sketch all possible paths and determine the edge corresponding to minimum cost path.

   (b) Obtain the 4 directional chain code and the shape number for the image shown below :— 10



[TURN OVER

4. (a) Obtain Huffman code for the word 'COMMITTEE'. **10**
   (b) For the 3 bit, 4 x 4 size image, perform the following operations :— **10**
   (i) Image Negative
   (ii) Intensity Level slicing with background with $\gamma_1 = 2$ and $\gamma_2 = 5$
   (iii) Bit Plane Slicing
   (iv) Thresholding
   (v) Clipping with $\gamma_1 = 2$ and $\gamma_2 = 5$.

0	7	3	1
3	6	4	6
2	4	2	2
1	2	5	3

5. (a) Draw and explain block diagram of JPEG Encoder and Decoder. **10**
   (b) For a given orthogonal matrix A and image U : **10**

$$A = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \qquad U = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix}.$$

Find transformed image and basis images.

6. (a) Explain method of segmentation of images by :— **10**
   (i) Region Groving
   (ii) Region Split and merge.
   (b) Explain the following morphological operations in terms of dilation and erosion operations Hit or Miss transformation, Opening and Closing. **10**

7. Write short notes on (any **four**) :— **20**
   (a) Homomorphic Filtering
   (b) 2D Wavelet Transform Filter Bank
   (c) Image Sampling
   (d) Polygonal Approximation and Signatures
   (e) Any one application of Image Processing.

3/6/2011

BE ETRX VII (Rev)
VLSI Design

Con. 3447-11. **(REVISED COURSE)** **RK-3336**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary**.

1. (a) Draw the stick diagram and mask layout using λ based design rules for a depletion load nMOS inverter with pull up to pull down ratio as 4:1 (i.e. $\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$). (10)

   (b) Assuming that the work function of the metal is smaller than that of a p-type semiconductor, pictorially depict the cross sectional view and energy band diagram for an n-channel MOS transistor under the following conditions: (10)

   (i) When the metal and semiconductor are shorted
   (ii) Flat band condition
   (iii) When the surface is depleted of carriers
   (iv) Onset of inversion at the surface
   (v) When the semiconductor surface is accumulated with majority carriers.

2. (a) Explain the complete fabrication process steps for a CMOS inverter using p-well process with the help of cross sectional diagrams for all important masking steps. (10)

   (b) Calculate the threshold voltage V_{T0} at V_{SB} = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: (10)

   Substrate doping, $N_A = 10^{16}/\text{cm}^3$
   Polysilicon gate doping, $N_D = 2 \times 10^{20}/\text{cm}^3$
   Gate oxide thickness, $T_{OX} = 500\ A^0$.
   Oxide interface fixed charge density, $N_{OX} = 4 \times 10^{10}/\text{cm}^2$

   Also calculate the ion implant dose necessary to change the threshold voltage from V_{T0} to V_T = -1 V and comment on the result.

3. (a) Implement the following Boolean function in CMOS logic: (10)
   $Y = \overline{A(D+E)+BC}$
   Draw the stick diagram for the circuit.

   (b) Derive an expression for the inverter threshold voltage (switching voltage) of a CMOS inverter. Calculate the (w/L) ratios of the nMOS and pMOS transistor in the CMOS inverter circuit with the following parameters: (10)

   NMOS $V_{Tn} = 0.6$ V, $\mu_{ncox} = 60\ \mu A/V^2$,
   PMOS $V_{Tp} = -0.8$ V, $\mu_{pcox} = 20\ \mu A/V^2$,
   $V_{DD} = 3$ V, $V_{TH} = 1.5$ V

4. (a) Compare Resistive load, Depletion load and Enhancement load inverters. Also write their merits, demerits and applications. (10)

   (b) Design a half adder circuit using primitive gates. Using the half adder blocks designed & required primitive gates, design a full adder circuit. Write verilog codes for both the circuits designed and a Test bench to test the functionality of the full adder. (10)

5. (a) Explain various sources of power dissipation in digital CMOS circuits with the help of appropriate diagrams and expressions. (10)

   (b) Consider an n-channel MOSFET with W = 15 μm, L = 2 μm and $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2. Assume that the drain current in the non saturation region for $V_{Ds} = 0.10$ is $I_D = 35$ μA at $V_{Gs} = 1.5$ V and $I_D = 35$ μA at $V_{Gs} = 2.5$ V. Determine the inversion carrier mobility and the threshold voltage of the n-MOSFET. (10)

6. (a) Explain constant voltage and constant field scaling in detail with their merits and demerits. (10)

   (b) Design a clocked SR latch using CMOS technology and write verilog code for the circuit. (10)

7. Write short notes on any three: (20)

   (a) CMOS latch up & its prevention
   (b) Buried and Butting contacts
   (c) Ion implantation
   (d) MOS capacitance .

BE CETRX VII (Rev)
Filter Design

Con. 3272-11. (REVISED COURSE) RK-3333

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data whenever **necessary** and **justify** it.

1. (a) Compare frequency response of Butterworth, Chebyshev (Type I and Type II) and Elliptical filters. **20**
(b) Explain the principle of switched capacitor filter.
(c) Compare FIR and IIR filters.
(d) Compare impulse invariant and bilinear transformation methods in IIR filter design.

2. (a) Mention design steps of Chebyshev filter. How it differs when "N" is odd and when "N" is even ? **10**
(b) Explain Gibb's Phenomenon. State its significance in FIR filter design. **10**

3. (a) Convert the analog filter with system function : $H_a(s) = \frac{s+0.1}{(s+0.1)^2+16}$ into a digital filter (IIR type) by means of the bilinear transformation. **20**

The digital filter should have a resonant frequency $W_r = \frac{\pi}{2}$.

4. (a) S.T. $S = \frac{2}{T}\frac{(1-z^{-1})}{(1+z^{-1})}$ in bilinear transformation. Also explain mapping between s – plane and z – plane for BLT. **10**
(b) For the given specification α_p = 3 dB, α_s = 15 dB; Ω_p = 1000 rad/sec and Ω_s = 500 rad/sec design a highpass filter. **10**

5. (a) Write Design steps of (FIR) Filter using Kaiser window. **10**
(b) Explain concept of adaptive filter and basic blocks required for its design. **10**

6. (a) Explain concept of Decimation Interpolation. **10**
(b) Determine the order and the poles of a lowpass Butterworth filter that has a 3 dB attenuation at 500 Hz and an attenuation of 40 dB at 1000 Hz. **10**

7. Write short notes on any **four** :– **20**
(a) Higher order filters
(b) Subband coding
(c) Applications of Weiner filter
(d) Step invariant method steps in the design of IIR filter
(e) Transfer function of 2nd order lowpass analog Butterworth filter.

BE ETRX VII CRev)
Power Electronic & Drives

Con. 3108-11. **(REVISED COURSE)** **RK-3348**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume suitable **data**, if any.

1. Attempt the following :— 20
   (a) With the help of block diagram, explain the operation of Online UPS system.
   (b) Explain Dynamic braking for D. C. motor.
   (c) What is time ratio control in D. C. choppers ? Explain the use of TRC for controlling the output voltage in choppers.
   (d) State the need of reduction of harmonics in inverter output.

2. (a) With the help of neat circuit diagram and waveforms, explain the operation of isolated forward converter. 10
   (b) Explain the effect of source inductance on the performance of a single phase fully controlled converter with neat diagrams and waveforms, indicating clearly the conduction of various thyristors during one cycle. 10

3. (a) Explain single pulse width modulation as used in PWM inverters. 10
   (b) With the help of circuit diagram and associated waveforms, explain the principle of working of two quadrant (class C) chopper. 10

4. (a) State the various methods of speed control of Induction motor. Discuss the stator voltage control method. 10
   (b) Describe the working of a single phase full converter fed D. C. separately excited motor with circuit diagram, relevant waveforms and expressions. 10

5. (a) Explain the slip power recovery control of three phase Induction motor. **10**

(b) A load commutated chopper, fed from a 230 V d. c. source has a constant load current of 50 A. For a duty cycle of 0·4 and a chopping frequency of 2 kHz, calculate :— **10**

(i) the value of commutating capacitance.

(ii) average output voltage.

(iii) circuit turn-off time for one SCR pair.

(iv) total commutation interval.

6. (a) Explain with diagram, the operation of series inverter. State its limitations. How these limitations are overcome ? **10**

(b) The speed of a separately excited D. C. motor is controlled by a semiconverter. The field current which is also controlled by a semiconverter is set to the maximum possible value. The A. C. input voltage is single phase, 208 V, 50 Hz. The armature resistance $R_a = 0{\cdot}25\ \Omega$, $R_f = 147\ \Omega$ and the motor voltage constant $K_v = 0{\cdot}7032$ V/A – rad/sec. The load torque is $T_L = 45$ Nm at 1000 rpm. Assume armature current to be continuous and ripple free, calculate :— (i) the field current I_f (ii) the delay angle of converter in armature circuit (α_a) **10**

7. Write short notes on the following :— **20**

(a) Parallel Inverter

(b) Dual Converter

(c) V/f control for Induction Motor.