BE | ETRX | VII CRev 27/5/13

Communication Networks

1st Half-13-Mina - (d)-4

Con. 8964-13. **(REVISED COURSE)** **GS-5743**

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Assume **suitable** data if **necessary**.

1. Attempt any **four** :— **20**
   (a) Give reasons for using layered protocols ?
   (b) Explain how microwave communication work.
   (c) Explain various LAN Topologies.
   (d) What is sliding window protocol ? Where it is applicable ?
   (e) Explain general principles of congestion control.

2. (a) Explain circuit switching, packet switching and message switching. **10**
   (b) Compare the performance characteristics of co-axial, twisted pair and fiber optic transmission media. **10**

3. (a) Explain in detail O.S.I. model. **10**
   (b) What is DSL technology ? Explain various DSL technologies and compare. **10**

4. (a) Draw the block diagram of SONET and explain its operation. Also explain SONET frames. **10**
   (b) State and explain various frame types in HDLC. **10**

5. (a) What is ethernet ? Explain fast ethernet specifications. Also explain CSMA-CD in detail. **10**
   (b) What are the different types of routing ? Explain link state routing. **10**

6. (a) Explain the following network connecting devices :— **10**
      (i) Switches (iv) hub
      (ii) Routers (v) Bridge.
      (iii) Gate way
   (b) Explain different ARQ techniques. **10**

7. Explain the following :—
   (a) TCP-IP Model **5**
   (b) Leased Line Concept **5**
   (c) ISDN **5**
   (d) Ipv4. **5**

14/5/13

BE (ETRX) SEM VII (REV) May 2013
Power Electronic & Drives.

D : PH (April Exam) 203

Con. 8344-13. **GS-5410**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume suitable data, if **any**.

1. (a) Explain constant torque and constant power drive methods with relevant diagram and waveforms. **5**
   (b) A single phase full converter is made to deliver a constant load current. For zero degree firing angle the overlap angle is 15°. Calculate the overlap angle when firing angle is 45°. **5**
   (c) Induction motor speed control with constant supply voltage and reduced supply frequency is rarely used in practice. Justify the statement. **5**
   (d) List the merits and demerits of online UPS and offline UPS. **5**

2. (a) With neat circuit diagram explain the working of a load commutated chopper with relevant voltage and current waveforms. Show voltage variation across each pair of SCR's as a function of time. **10**
   (b) Describe modified Mc-Murray Bedford half bridge inverter circuit with related voltage and current waveforms. **10**

3. (a) Explain with neat diagram the working of parallel inverter employing feedback diodes. Draw the voltage and current waveforms. What care should be taken to avoid commutations failure ? **10**
   (b) A 220 V, 1000 rpm, 60A separately excited D.C. motor has an armature resistance of 0·1Ω. It is fed from a single phase full converter with an a.c. source voltage of 230V, 50Hz. Assuming continuous conduction, compute. **10**
      (i) firing angle for rated motor torque at 600 rpm.
      (ii) firing angle for rated motor torque at (– 500) rpm.
      (iii) motor speed for $\alpha = 150°$ and half rated torque.

4. (a) Draw and explain the power circuit of semiconverter feeding a separately excited D. C. motor. Explain with typical voltage and current waveforms the operation in both continuous and discontinuous armature current modes. **10**
   (b) Draw the circuit diagram and explain the rotor resistance control method using chopper for the speed control of 3 phase induction motor. **10**

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5. (a) Explain with relevant circuit diagrams the static scherbius drives for obtaining speeds below as well as above synchronous speeds. **10**

   (b) State the need for reduction of harmonics in inverters. Outline the various methods for reduction of harmonics. Explain how harmonic reduction using stepped wave inverters is done. **10**

6. (a) With the help of circuit diagram and waveforms, explain the operation of isolated flyback converter in discontinues mode. Also state the advantages and disadvantages. **10**

   (b) A current commutated chopper is fed from a d.c. source of 230 V. Its commutating components are L = 20 μH and C = 50 μF. If load current of 200 A is assumed constant during the commutation process then compute. **10**

   (i) Turn off time of main thyristor

   (ii) total commutation interval

   (iii) Turn off time of auxiliary thyristor.

7. Write short notes on :–

   (a) Dual converter **7**

   (b) PWM inverter **7**

   (c) Step up chopper **7**

BE | ETRx | VII (R) 21/5/13
VLSI Design

Con. 8903–13. **GS–5530**

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any questions **four** out of remaining **six** questions.
(3) Assume suitable **data** wherever **necessary** and state it **clearly**.

1. Attempt any **four** :– **20**
   (a) Discuss why the threshold voltage changes when a reverse-biased source-to-substrate voltage is applied to a MOSFET.
   (b) Consider on MOS structure with a p-type semiconductor substrate doped to $N_a = 10^{16}/cm^3$, a silicon dioxide insulator with a thickness of 500 A°, an n^+ polysilicon gate doped to $2 \times 10^{20}/cm^3$ and oxide-interface charge density of $4 \times 10^{10}/cm^2$ calculate the flat band voltage.
   (c) Explain the λ(lambda) based design rule for an implant mask in nMOS technology and the problems faced in case of violation of the rule during fabrication. Draw appropriate diagrams.
   (d) Discuss various steps of Silicon Planar Process and its advantage in fabrication of Integrated circuits.
   (e) Design a 4:1 MUX using nMOS pass transistor logic and discuss the drawbacks of the circuit and the remedies to overcome the drawbacks.

2. (a) Sketch and explain the general shape of the low frequency C-V characteristics to be expected from a metal-oxide-p-substrate capacitor. How does the characteristic change for the high frequency condition ? **10**
   (b) Consider an n-channel MOSFET with gate width w = 10μm, gate length L = 2μm, and oxide capacitance $C_{ox} = 10^{-7}$ F/cm². In the linear region, the drain current is found to have the following values at $V_{DS} = 0.1V$: **10**
   $I_D = 50\ \mu A$ at $V_{GS} = 1.5$ V
   $I_D = 80\ \mu A$ at $V_{GS} = 2.5$ V
   Calculate the inversion carrier mobility and the threshold voltage of the device.

3. (a) What do you mean by inverter ratio ? Derive the same for a CMOS inverter and discuss symmetric CMOS inverter design. **10**
   (b) A PMOS transistor is to be fabricated. Describe its fabrication steps giving the mask sequence. Sketch the cross sectional view of all the masking steps. **10**

4. (a) Draw the stick diagram and mask layout using λ based design rules for a depletion load nMOS inverter with pull-up to pull-down ratio as 4:1 $\left(\text{i.e.}\frac{z_{pu}}{z_{pd}} = \frac{4}{1}\right)$ **10**

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(b) Determine the device sizes for 3-input NAND and 3-input NOR gates in conventional CMOS. Assume that the basic inverter is sized as $\left(\frac{W}{L}\right)_n = 1$, $\left(\frac{W}{L}\right)_p = 2$ and the goal of the design is to have NAND 3 and NOR 3 gates with the same delay characteristics as the inverter. What problems arise if the number of fanins (inputs) is increased to 10 ?

5. (a) Compare the full scaling model with constant voltage scaling model for MOSFETS. Demonstrate clearly the effects of scaling on the device density, speed of the circuit, power consumption and current density of the gates. 10

(b) A depletion load nMOS inverter has following parameters : 10

$\mu n C_{ox} = 30\ \mu A/V^2$, $V_{TO} = 0{\cdot}8V$ (enhancement type)

$V_{TO} = -2.8V$ (depletion type), $r = 0.38\sqrt{V}$

$|2\phi_f| = 0.6V$, $V_{DD} = 5V$

(i) Determine the $\left(\frac{W}{L}\right)$ ratios of both transistors such that the static power dissipation for $V_{in} = V_{OH}$ is 250 mW, and $V_{OL} = 0.3V$.

(ii) Calculate V_{IL} and V_{IH} values and determine the noise margines.

6. (a) Implement the circuit for clocked SR-latch at switch level and write verilog module for the circuit designed. 10

(b) Implement the following function using CMOS technology $F=\overline{XYZ+XW}$. Also draw the stick diagram for the circuit designed. 10

7. Write short notes (attempt any **two**) :– 20

(a) 4 × 4 barrel shifter

(b) Short channel effects

(c) CMOS latch-up and its prevention.

BE/ETRX/VII (R·) 31/5/13
Wireless Communication

mk.94-1st hlf 13-K

Con. 9891-13. **GS-4999**

(OLD COURSE)

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Solve **one complete** question **together**.

1. (a) Derive the relation $Q = \sqrt{3N}$ where Q is co-channel re-use ratio, N is cluster size. **20**
   (b) Explain the need of umberlla cell approach.
   (c) Explain orthogonal covering in CDMA.
   (d) Differentiate between Erlang-B and Erlang-C system of trunked radio.

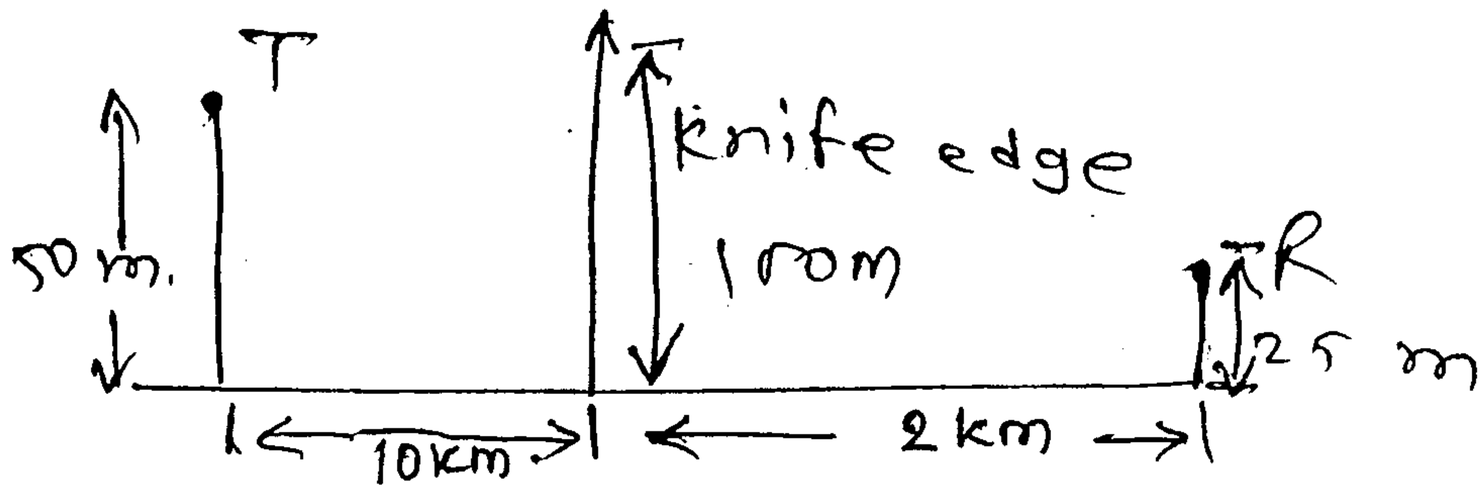
2. (a) Explain the different techniques to increase coverage area and capacity. **10**
   (b) Explain the frame structure in GSM along with different bursts format. **10**

3. (a) Draw and explain GSM system architecture along with different interfaces. **10**
   (b) Using two-ray ground reflection model, derive the relation for the $E_{TOT}(d)$ at a distance d from the transmitter antenna. **10**

4. (a) Differentiate between Flat fading and Frequency selective fading. **5**
   (b) Explain diffraction with the help of Fresnel Zone Geometry. **10**
   (c) Explain the need of spreading the sequence in CDMA. **5**

5. (a) With the help of neat block diagram explain Amps voice modulation process. Explain use of SAT and ST tones. **10**
   (b) With the help of neat block diagram explain forward CDMA channel modulation process. **10**

6. (a) For the given geometry determine — **10**
   (i) the loss due to Kinfe-edge diffraction
   (ii) the height of the obstacle required to induce a 6-dB diffraction loss. Assume f = 900 MHz.



   (b) List of different control channels in detail along with their uses in GSM. **10**

7. Write short notes on :— **20**
   (a) RAKE Receiver
   (b) DECT system
   (c) GPRS
   (d) Log-normal shadowing.