Power Electronico & Dince

BEETRX SEN VII

OP Code · MW-200a

| riay | 2014 | QI Code, IVI V-2.009,9 | | |
|--------|---------------------------------------|---|----------|--|
| | | (3 Hours) [Total Marks: | ks:100 | |
| | (2) Atte (3) Fig | estion No. 1 is compulsory. Empt any four questions out of the remaining six questions. ures to the right indicate full marks. ume suitable data wherever requried but justify it. | | |
| 1. An | swer the (a) (b) (c) (d) | Compare symmetrical and asymmetrical semi-converter. What is meant by voltage commutation and current commutation. Compare series and parallel inverter. What is four quadrant DC - drive. | 20 | |
| | A load current Calcula (i) (ii) (iii) | Value of commutating capacitor. Average output voltage. Circuit turn off time for 1-pair of SCRs. | 10 | |
| • | and wa Explain | the working of a single phase series inverter with appropriate circut veforms. I constant torque and constant power operation of separately excited tor. Give schematic diagram of control unit. | 10 10 | |
| 4. (a) | | le plase fully controlled bridge with 230 V, 50 HZ supply feeds tous ripple free current of 20A. If $L_s = 2.5$ mH. Calculate overlap angle for firing angle 60°. | 10 | |

- What will be the new value of overlap angle for same firing angle if (ii) load is reduced by 50%.
- (b) Draw and explain the variable voltage and variable frequency control method for 3-phase squirrel cage induction motor. What is the significance of (V/F) ratio control.
- (a) A single phase full converter is used to drive separately excited dc shunt motor with $R_a = 0.25 \Omega$. Motor rating are 220 V, 750 rpm, 50 A. If input voltage to converter connected to armature is 250 V a.c. 50 Hz. Calculate:-
 - Firing angle delay for 500 rpm at rated torque.
 - Speed of motor for firing angle $\alpha = 60^{\circ}$ at half load.
 - (b) Explain the working of Jone's chopper with the help of various waveforms. 10

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QP Code: MV-20099

VLSI Design, -ETRX-SemvII(R). 04/06/14 May-June-14.

QP Code: MV-20169

(3 Hours)

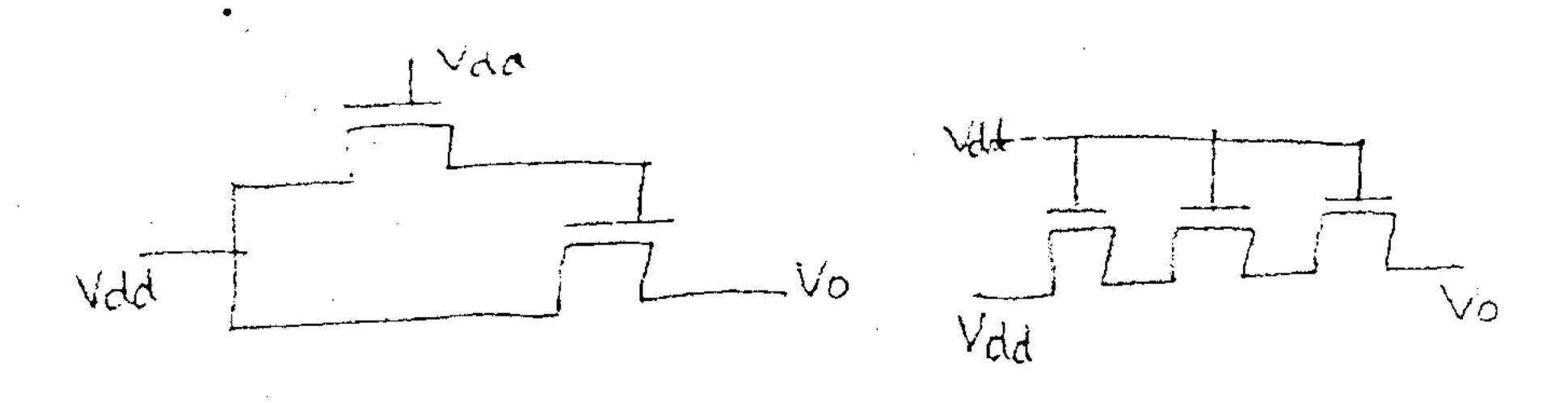
Total Marks: 100

N. B.: (1) Question no. one is compulsory.

- (2) Solve any four questions from remaining questions.
- (3) Draw neat diagrams wherever required.
- 1. Answer the following questions (write any 4).

20

- (a) The segregation coefficient of O_2 is 0.25. Find the concentration of oxygen in the silicon ingot at a fraction solidified of 0.3. The concentration of O_2 in the silicon at the top of the crystal is 12.5×10^{17} atoms/cm³ at a fraction solidified of 0.1?
- (b) Draw the schematic, stick diagram of a NMOS depletion load inverter?
- (c) Explain what is pass transistor logic? Calculate the output voltage for the following circuits if Vdd = 5V and Vth = 1.5 V.



- (d) Define threshold voltage with equation and explain body effect?
- (e) State the difference between diffusion and ion implantation?
- 2. (a) With neat cross sectional diagram explain the process of CMOS fabrication 10 using pwell process. Thus given the number of masks required.
 - (b) Consider on aluminium silicon dioxide silicon MOS structure with the following parameters.

$$N_d = 2.5 \times 10^{14}/\text{cm}^3$$
 $Q_{ox} = 10^{10} \text{ cm}^2$
 $T_{ox} = 650 \text{ A}^\circ$
 $\phi_{ms} = -0.35 \text{ V}$

Given
$$n_i = 1.45 \times 10^{10}/\text{cm}^3$$
, $\epsilon_o = 8.85 \times 10^{-14}$

$$\varepsilon_{\rm si} = 11.7, \ \varepsilon_{\rm ox} = 3.97 \varepsilon_{\rm o}$$

Determine the threshold voltage of the device.

- 3. (a) Draw the circuit diagram of two input NAND gate using CMOS. Draw its stick diagram and layout using λ based rules.
 - (b) State all types of inverters and compare them with their merits, demerits and applications.
- 4. (a) Determine pullup to pulldown ratio $\left(\frac{Zpu}{Zpd}\right)$ for an NMOS inverter driven 10 by another NMOS inverter?
 - (b) Explain latchup condition in CMOS in detail. What are the remedies to avoid latchup?
- (a) A CMOS logic gate that implements the function.
 F = X · (Y + Z) + X · W
 is needed in a control network. Design the logic circuit and draw the stick diagram using Euler's method?
 - (b) Design 4:1 MUX using CMOS transmission gate logic. Draw the stick diagram of the same design?
- 6. (a) Compare both the scaling methods? Show analytically how power dissipation, 10 maximum operating frequency, current density and saturation current scale in terms of scaling factors?
 - (b) Write switch level verilog code for a 2 input NAND gate. Using the module of NAND gate, design SR-Latch and write the switch level verilog code for the same.
- 7. Write short notes on any two:
 - (i) Short channel effects in MOSFETs
 - (ii) Comparision of burried and butting contacts.
 - (iii) Semicustom and Full custom design.

QP Code: MV-20034

| | (3 Hours) | [Total Marks: 10 | 0 |
|-------------|---|---------------------|-------------|
| N.] | B.: (1) Question No. 1 is compulsory. (2) Attempt any four out of the remaining six questions. (3) Assume suitable data if requried. (4) Figures to the right indicate full marks. | | |
| 1. | (a) What is mobile assisted Hand off? Explain strategy.(b) Explain orthogonal covering in CDMA.(c) What is macro-cell zone concept?(d) Explain spectral efficiency and pulse shaping in OFDM? | | 5 5 5 |
| 2. | (a) Draw a neat block diagram for signal processing in GSM at (b) Explain with architecture:- (i) High speed circuit switched data in GSM. (ii) General Packer Radio Services (GPRS). | | 0 |
| 3. | (a) Explain the need of spreading the sequence in CDMA. transmitter and Receiver with neat block diagram. (b) Explain MAC sub layer of CDMA 2000 in detail. | | 0 |
| 4. | (a) Explain OFDM block diagram and derive the mathematic OFDM signal.(b) Explain in detail the working of RAKE receiver. | | 0 |
| 5. | (a) Explain the Authentication, Cipher key generation and Encrops GSM. (b) Prove that far a hexagonal geometry, the co-channel representation of the provention of the co-channel representation. (b) Prove that far a hexagonal geometry, the co-channel representation of the co-channel representation. (c) Prove that far a hexagonal geometry, the co-channel representation of the co-channel representation. (d) Prove that far a hexagonal geometry, the co-channel representation of the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (e) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove that far a hexagonal geometry is proved the co-channel representation. (f) Prove the co-channel representation is proved the co-channel representation. (f) Prove the co-channel representation is proved the co-channel representation. (f) Prove the co-channel representation is proved the co-channel representation. (f) Prove the co-channel representation is | se ratio is given 1 | - |
| 6. | (a) Explain different security. Algorithms for GSM.(b) Explain CDMA channel modulation process with the hediagram. | | 0 |
| 7. | Write short notes on any three: (a) Subscriber identity module. (b) Bluetooth. (c) WiMAX. (d) Zigbee. | 2 | 20 |