B.E. sem. VII (old) ENTRY → 31/05/2016

VLSI Design

**QP Code : 29908**

(3 Hours) [Total Marks : 100

**N.B.-** (1) Question No. **1** is **Compulsory.**
(2) Attempt any **Four** out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary.**

1. Answer any **FOUR.** (20)
   (a) Define threshold voltage of an enhancement and depletion type MOSFET. What is the effect of substrate bias on threshold voltage of the device?
   (b) Differentiate between the process of ion implantation and diffusion in fabrication of a MOS transistor.
   (c) Construct a 2 X 2 array multiplier circuit and write a verilog module for your design.
   (d) Find the flat band voltage of a MOS capacitor with substrate doping concentration of $10^{16}/cm^3$ and silicon dioxide thickness of 500A°. Assume $Q_{OX} = 10^{11} q/cm^2$ and $\varphi_{ms} = -1.1 V$.
   (e) Explain the effect of full scaling and constant voltage scaling on current density and delay in a MOSFET.

2. (a) Assuming that the work function of the metal is smaller than that of the p-type semiconductor, pictorially depict for an n-channel MOS transistor, the energy bands and Fermi level in the semi conductor, conduction band in the oxide, Fermi level in metal under the following conditions : (10)
      i. Flat band condition
      ii. Onset of inversion at the surface.
      iii. When the surface is depleted of carriers.
      iv. When the metal and semiconductor are shorted.
   (b) An enhancement mode n-channel MOSFET has the following parameters. (10)
   Threshold voltage $V_T = 0.8$ V, Channel length modulation coefficient $\lambda = 0.05/V$, $\mu_n C_{ox} = 20\ \mu A/V^2$, $W/L = 20$
   Find the drain current for the following cases.
      (i) $V_g = 5$ V, $V_D = 4$ V, $V_S = 2$ V
      (ii) $V_g = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V

3. (a) What do you mean by inverter ratio? Derive the same for depletion load nMOS inverter which is driven by another similar inverter. (10)
   (b) Implement the following Boolean function in CMOS logic: (10)
   $$Y = \overline{(AB + AC) + (AD)}$$
   Draw the optimized stick diagram of the logic gate using Euler path.

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4. (a) An nMOS transistor is to be fabricated. Describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. (10)
   (b) Sketch and explain the CV characteristics of MOS capacitor with n- type substrate under low frequency conditions. How does the characteristic change under high frequency condition? (10)

5. (a) Draw the schematic diagram, stick diagram and mask layout of a CMOS inverter using $\lambda$ based design rules. (10)
   (b) Implement a 2:1 multiplexer circuit using CMOS transmission gates. Write a Verilog module for the circuit at switch level of abstraction. Write a test bench to check the functionality of the circuit. (10)

6. (a) Explain various sources for power dissipation in digital CMOS circuit. (10)
   (b) Draw the p-well CMOS inverter and explain the latch up effect in it. What are the remedies to avoid the latch up problem in the circuit? (10)

7. Write short notes on any **two**: (20)
   (a) Short channel effects
   (b) Design rules and their necessity
   (c) Comparison of types of loads in NMOS inverters

BE. Sem. VII 2019 Old CBSGS
Wireless communication

**QP Code : 29762**

(3 Hours)

[Total Marks: 100]

N.B. (1). Question No. 1 is compulsory.
(2). Solve any four questions out of the remaining six questions.

1. (a) Explain Umbrella Cell approach in cellular system. (20)
(b) Explain the difference between Soft hand off and Hard hand off.
(c) Explain GoS (Grade of Service).
(d) Explain Spectral efficiency and pulse shaping in OFDM.

2. (a) Explain cdma 2000 layered architecture. Also explain MAC and LAC sub layers. (10)
(b) Explain GSM system architecture with interface. (10)

3. (a) Explain the need of spreading the sequence in CDMA. Also explain DS-SS transmitter and receiver with neat block diagram. (10)
(b) Explain OFDM block diagram and derive the mathematical expression for OFDM. (10)

4. (a) Explain the different techniques to increase coverage area and capacity. (10)
(b) Explain the architecture of GPRS system. Also explain the functionalities of SGSN and GGSN nodes. (10)

5. (a) A 30 MHz total spectrum is allocated for a duplex wireless cellular system and each simplex channel has 30 KHz RF bandwidth. Find:- (10)
(i) the no. of duplex channels available.
(ii) the total no. of channels per cell site, if N=4 and N=7.
(b) Explain the need for power control in CDMA. How is it implemented? (10)

6. (a) Explain different traffic channels and control channels in GSM. (10)
(b) Explain uplink and downlink CDMA (IS-95) models. (10)

7. Write short notes on: - (20)
(a) ZigBee
(b) Security in GSM
(c) Rake Receiver
(d) Bluetooth

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