Sem VII CBGS
Electronics

QP Code : 728800

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question no. **1** is **compulsory**
(2) Solve any three from the remaining five questions
(3) Assume suitable data if necessary.
(4) **Figures** to the **right indicate** full **marks.**

1. Attempt **any four** of the following. **20**
   (a) Differentiate between an artificial neural network and a digital computer.
   (b) What are excitatory and inhibitory weighted interconnections?
   (c) Differentiate between supervised and unsupervised learning.
   (d) What is a membership function?
   (e) Explain the delta rule of learning with an example.

2. (a) With the help of a flow chart, explain Single Continuous Perceptron Training Algorithm. **10**
   (b) Implement the perceptron learning rule for the following set of input training vectors: **10**
   $X_1 = [1\ -1\ 0\ 1]^t$; $X_2 = [0\ 1.5\ -0.5\ -1]^t$; $X_3 = [-1\ 1\ 0.5\ -1]^t$
   The learning constant, c = 0.1 and the desired responses for X_1, X_2 and X_3 are $d_1 = -1$, $d_2 = -1$ and $d_3 = 1$ respectively. Assume the initial weight vector to be $W^1 = [1\ -1\ 0\ 0.5]^t$ and obtain the updated weight vector after one epoch.

3. (a) With the help of a flow chart, explain error back propagation algorithm. **10**
   (b) Give the network architecture of an Adaline network and discuss its training procedure. **10**

4. (a) What are Discrete Hopfield Networks? Explain how patterns are stored in them. **10**
   (b) With a neat architecture, explain the training algorithm of Kohonen self-organizing feature maps. **10**

5. (a) Two fuzzy sets are defined as: **10**

$$\underset{\sim}{A} = \left\{\frac{1}{2} + \frac{0.3}{4} + \frac{0.5}{6} + \frac{0.2}{8}\right\}$$

$$\underset{\sim}{B} = \left\{\frac{0.5}{2} + \frac{0.4}{4} + \frac{0.1}{6} + \frac{1}{8}\right\}$$

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Perform union, intersection, difference and complement over these fuzzy sets.

(b) Explain any four defuzzification methods with suitable diagrams. **10**

6. Write short notes on **any four**: **20**
   (a) Learning factors
   (b) Perceptron convergence theorem
   (c) Adaptive Resonance Theory
   (d) Hebbian learning
   (e) Adaptive neuro-fuzzy infonnation systems

BE (ETRX) CBSGS

IC Technology

19/5/2017

Q. P. Code: 11130

(2)

Time: 3 Hours.

Max. Marks: 80

N.B. 1) Question No. 1 is compulsory.
2) Solve any three questions from the remaining questions.
3) Assume suitable data if necessary.

1. Solve any four of the following. (5 marks each) (20)

(a) What is the significance of High K and Low K dielectric in CMOS process?
(b) Explain the difference between contact, proximity and projection printing?
(c) Describe the SIMOX method for fabrication of SOI.
(d) Enlist the steps for obtaining Silicon from Sand.
(e) Explain the difference between Positive Photo resist and Negative Photo Resist.

2. (a) Explain Float zone method for Silicon crystal growth. What are its advantages? (10)
(b) Classify the types of Thin Film Deposition methods. (04)
(c) Explain the LPCVD process with neat diagram. Also enlist its advantages (06)

3. (a) Enlist the steps for fabrication of CMOS inverter using twin tub process. Draw vertical cross-sectional views starting from the substrate till the gate and source and drain formation in the fabrication of CMOS inverter using twin tub process. (10)
(b) Draw layout of CMOS NOR gate along with its circuit diagram. (05)
(c) Explain buried and butting contact. (05)

4. (a) Explain Steps of Lithography with suitable diagrams. Also classify Lithography techniques. (10)
(b) What is LOCOS? Why it is required in the CMOS process. Explain technology solutions for avoiding problems in LOCOS. (10)

5. (a) Describe with the help of a neat diagram Hayness-Schokley experiment for measurement of Drift Mobility of n-type semiconductor. (10)
(b) Explain Deal Groove model for Oxidation process. Explain where dry and wet oxidation processes are used during MOSFET fabrication process. (10)

6. Write short notes on any four of the following. (5 marks each) (20)

(a) FINFETs
(b) Automatic Test equipment
(c) Hall effect and resistivity measurement.
(d) BiCMOS
(e) Fabrication of carbon nanotube transistor.

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B.E. Sem-VII (Electronics) CBSGS 15/05/2017 (53)
Embedded System Design

Q.P.Code: 013691

(3 Hours) **[Total Marks: 80]**

1) Question no. 1 is compulsory
2) Solve any three from the remaining five questions.
3) Assume suitable additional data if necessary.

Q1 Answer the following questions. (20)

a) Justify the need for brown-out detection circuit in embedded systems environment and the mechanism of implementing the same.
b) What is a watch-dog timer, its use and typical application for an embedded system.
c) Explain the structure of typical C source program for ARM based target processor. Typically list the various data types along-with memory size supported by a C compiler.
d) Compare the serial communication protocols RS – 232C and RS – 485 protocols.

Q2 a) Write a note on the interrupt structure of Cortex – M architecture. (10)

b) Explain the utilisation bound in task scheduling in light of Rate Monotonic Scheduling algorithm. (10)

Q3) a) What is a task and various states that a task can lie in for an embedded environment. (10)

b) Explain briefly the register structure of Cortex-M3 architecture along-with the function of various special registers. (10)

Q4 a) Compare the features of Cortex – A8 and Cortex - R4 architectures. (10)

b)Explain the operation and significance of following MicroC/OS – II functions

a) OSSemPend(); & OSSemPost(); b) OSMboxPost(); & OSMboxPend(); (10)

Q5) a)Write a brief note on boundary scan architecture. (10)

b) Explain the various inter- process/task communication and synchronisation tools like semaphores, mutex, mailbox and pipe used by an RTOS environment. (10)

Q6) Write short notes on (Any two) (10 x 2) (20)

a) Problem of priority inversion and mechanism to prevent the same.
b) MSP-430 architecture and its low power capability.
c) Design metrics for a typical embedded system.

BE ETRX I VII VD

1/06/17

(02)

Q. P. Code : 10831

(3 Hours) **(Total Marks : 100**

N.B.: (1) Question No. **1** is **Compulsory**.
(2) Attempt any **Four** out of remaining **six** questions.
(3) Assume **suitable** data wherever **necessary**.

1. Answer any **FOUR.** (20)
   (a) Explain velocity saturation effect in a long channel MOSFET. How does it affect the current in a short channel device?
   (b) "NMOS pass transistor cannot pass strong logic 1". Justify the statement.
   (c) Draw the schematic and stick diagram of 2 input NAND gate in CMOS technology.
   (d) Differentiate between the process of ion implantation and diffusion in fabrication of a MOS transistor.
   (e) Design a 2:1 MUX using transmission gate logic and write a verilog module for the circuit designed.

Q.2. (a) MOS system that is characterized by $t_{OX} = 200A^{o}$ and $N_A = 10^{15}$ /cm^3. An n- type poly gate is used with $N_{d,poly} = 2X10^{19}$/cm^3. The fixed oxide charge is approximated as $Q_{OX} = q\ (10^{10})$ C/cm^2 and is the dominant oxide charge term. Calculate the flat band voltage, the threshold voltage before a threshold ion implant and the value of the acceptor ion implant dose N_I needed to set V_{T0} to 0.7V. (10)

(b) Explain the working principle and I-V characteristics of an n- channel enhancement type MOSFET with the help of appropriate diagrams. (10)

Q.3. (a) Plot the voltage transfer characteristics of a depletion load NMOS inverter and derive the expressions for critical voltage points. What is the impact of increase in K_R value on the characteristics? (10)

(b) Implement the following Boolean function in CMOS logic: (10)

$$Y = \overline{(D + E + A)(B + C)}$$

Draw the optimized stick diagram of the logic gate using Euler path.

Q.4. (a) An nMOS transistor is to be fabricated. Describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. (10)

(b) Describe the hot electron and short channel effects in a MOSFET and explain how they affect the device characteristics. (10)

Q.5. (a) Draw the schematic diagram, stick diagram and mask layout of a CMOS inverter with K_R=1 using λ based design rules. (10)

(b) Explain various sources for power dissipation in digital CMOS circuit. (10)

Q.6. (a) Design a clocked SR latch using CMOS technology and write verilog code for the circuit. (10)

(b) Compare both the scaling methods. Show analytically how power dissipation, maximum operating frequency, current density and I_{dss} is affected in terms of scaling factors. (10)

Q.7. Write short notes on **any two**: (20)
   (a) Buried and Butting contacts
   (b) MOS capacitance
   (c) CMOS latch up & its prevention
