BharatiyaVidyaBhavan's

Sardar Patel Institute of Technology

(Autonomous Institute Affiliated to University of Mumbai)

Revision: SPIT-4-19

Bachelor of Engineering/Technology (B.E./B.Tech)
in
Electronics Engineering

Final Year Engineering
(Sem. VII and Sem. VIII)
Effective from Academic Year 2019 -20

Board of Studies Approval: 06/12/2018 & 26/04/2019

Academic Council Approval: 16/01/2019 & 15/05/2019

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Choice Based Internship Policy Details

Category '1':

Students who want to **register for placement and interested in joining semester long internship** will have following procedure

1. They will follow the regular placement procedure during their 7th Semester
2. They will proceed for internship in the company in which they have been selected from the next January.
3. Their credit requirements of 8th semester will be completed at the end of the **'summer term'** of their semester 6th.
4. The semester long internship will have credits assigned to it with appropriate evaluation mechanism.
5. The detail credit structure for semester 8thof category '1' will be declared in their next term in Jan 2019.

Category '2':

Students who do not want semester long internship (i.e. would want to continue with their **higher education immediately** after their B.Tech./B.E. program).

1. The normal semester 7th and 8th will be working for them as per their regular academic calendar
2. The detail credit structure for semester 8 of category '2' will be declared in their next term in Jan 2019.
3. Students will be allowed to participate for the placement in normal company.

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Choice of Category '1' or '2' shall be taken from the students in the mid of SEM VI.

Category '1': Student chooses for institute offered internship:

In this case student attends 'Summer Term' of 6 weeks duration.

Internship should be done by the student from 15th January to 30th June.

All the courses shall run twice a week during 'Summer Term'. Thus 1 hour lecture should be conducted for 12 hours in a summer term to get 1 credit.

ESE for summer term open elective courses shall be conducted in first and second week of July.

Make-up Examination for open elective courses shall be conducted along with SEM VI Make-up Examination.

Category '2': Student opt out of 'Institute offered company internship'

Student attends normal regular semesters as per institute calendar

SEM VIII students will attend OE courses along with SEM VI students.

Student appears for regular ESE examination.

Make-up Examination shall be conducted in first and second week of July.

Internship Related Other Guidelines:

1. Once a particular 'Category' is selected by the student then he/she will **NOT be allowed to change the category** for whatsoever reason.

2. If performance of the student is reported as poor by the industry or industry raises concerns about attendance issues of student during the internship then student may be called back to the institute. In this case he/she will have to complete the coursework equivalent to internship credits. If institute runs 'summer term' then student can take courses (two theory courses and two labs)

in summer term. Otherwise student will have to take courses (two theory courses and two labs) in the ODD semester of the next academic year. In this case student will be allowed to sit for the placement after rejoining the institute.

3. Internships will be given by the S.P.I.T. as per the selection criteria of company. Following are the other avenues for internships:

a. SPTBI

b. Reputed organizations like IIT, BARC, TIFR etc.with condition that the organization selected is ready to do the assessment for 10 credits of internship

c. If student get an internship offer on his own in a particular company then he/she needs to connect company.

4. For all internships, S.P.I.T. approval is must and there should be a grade penalty for students accepting internship and not joining a company or joining a company but not completing internship.

MOOC courses can be taken any time during the entire academic year. However MOOC* credits will be added to semester VIII as and when 'pass' certificate is submitted by the student.

List of MOOC courses will be curated by the department and students need to select from the list. If student wish to have course which is not present in the list then written approval from HoD and Dean Academics is necessary.

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Electronics Engineering Department

Semester VII common to both category '1' and category '2'

Student choose either A or B electives track

SEM VII						
Course Code	**Course Name**	**Group**	**Teaching Scheme (Hrs/week)**			**Credits**
			L	**T**	**P**	**Total**
ELE71^	Elective-I	PE	3	--	--	3
ELE72^	Elective-II	PE	3	--	--	3
ELE73^	Elective-III	PE	3	--	--	3
ELEL71^	Elective-I Lab	PE	--	--	2	1
ELEL72^	Elective-II Lab	PE	--	--	2	1
ELEL73^	Elective-III Lab	PE	--	--	2	1
ELP71	Category-'1': Major Project-II Category-'2': Major Project-I	PR	--	--	10#	5
CEP5	Problem solving module-V (Optional)	CEP				
	Total		9	--	16	17

Student choose either A or B electives track from ELE71 and ELE72. Any one course from ELE73A or ELE73B can be taken.

ELE71A	IC and MEMS Technology
ELE71B	Digital Signal Processing
ELE72A	Analog CMOS VLSI Design
ELE72B	Image Processing and Applications
ELE73A	Photovoltaic systems and Smart Grid
ELE73B	Computer and Communication Networks

Summer Term for Category '1': Student chooses for semester long internship

Summer Term						
Course Code	**Course Name**	**Group**	**Teaching Scheme (Hrs/week)**			**Credits**
HSS81	Technology Entrepreneurship Lab	HSS	--	--	2	1
OE^	Open Elective @	OE	1@	--	2@	2@
OE^	Open Elective @	OE	1@	--	2@	2@
ELP81	Category-'1': Major Project-I	PR	--	--	10	5
MOOC	MOOC (Min 8 week course)	MOOC	--	--	--	2
INT	Internship	PR	--	--	--	10#
ABL5	Financial Planning, Taxation Policies and Investment (Noncredit)	--	--	--	--	--
	Total		2	--	12+4@	8+4@+10#

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Semester VIII for Category '2':Student opt out of 'Semester Long Internship'

SEM VIII						
Course Code	**Course Name**	**Group**	**Teaching Scheme (Hrs/week)**			**Credits**
HSS81	Technology Entrepreneurship Lab	HSS	--	--	2	1
OE^	Open Elective @	OE	1@	--	2@	2@
OE^	Open Elective @	OE	1@	--	2@	2@
ELP81	Category-'2': Major Project-II	PR	--	--	10	5
MOOC	MOOC (Min 8 week course)	MOOC	--	--	--	2
ABL5	Financial Planning, Taxation Policies and Investment (Noncredit)	--	--	--	--	--
ELE81^	Elective-IV	PE	3	1		4
ELE81^	Elective-V	PE	3	1		4
ELEL81^	Elective-IV Lab	PE			2	1
ELEL81^	Elective-V Lab	PE			2	1
	Total		6+2@	2	16+4@	18+4@

Student can choose any two courses from the following as Elective-IV and Elective-V

A: Mixed Signal VLSI Design*
B: Neural Network and Fuzzy Logic Systems+
C: Electronic System Design
D: Radiating Systems

* Only for students who have opted for TRACK 'A' in SEM: VII. (Pre-requisite: ELE72A-Analog CMOS VLSI Design)
+ NOT for the students who have studied/opted for open elective course 'Introduction to Computational Intelligence'.

List of Open Elective Courses:

OE1: Consumer Electronics (ETRX)
OE2: Robotic Vision (ETRX)
OE3: Cyber Security and Digital Forensics (EXTC)
OE4: Internet of Things (EXTC)
OE5: Fundamentals of Computational Intelligence (COMP)
OE6: Fundamentals of Data Structures and Algorithms (COMP)
OE7: Software Testing (IT)
OE8: Database Management Systems (IT)

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Evaluation Scheme

B.E. Electronics Engineering (SEM VII)					
Course Code	**Course Name**	**Marks**			
		ISE	**MSE**	**ESE**	**Total**
ELE71^	Elective-I	20	20	60	100
ELE72^	Elective-II	20	20	60	100
ELE73^	Elective-III	20	20	60	100
ELEL71^	Elective-I Lab	40	--	--	40
ELEL72^	Elective-II Lab	40	--	--	40
ELEL73^	Elective-III Lab	40	--	--	40
ELP71	Category-'1': Major Project-II Category-'2': Major Project-I	80&	--	20	100
CEP5	Problem solving module-V (Optional)	--	--	--	--
	Total				**520**
For Category '2': B.E. Electronics Engineering (SEM VIII)					
Course Code	**Course Name**	**Marks**			
		ISE	**MSE**	**ESE**	**Total**
HSS81	Technology Entrepreneurship Lab	40	--	--	40
OE^	Open Elective @	40	10	20	70
OE^	Open Elective @	40	10	20	70
ELP81	Category-'2': Major Project-II	80**&**	--	20	100
MOOC	MOOC (Min 8 week course)	--	--	--	100
ABL5	Financial Planning, Taxation Policies and Investment (Noncredit)	--	--	--	--
ELE81^	Elective-IV	20	20	60	100
ELE81^	Elective-V	20	20	60	100
ELEL81^	Elective-IV Lab	40	--	--	40
ELEL81^	Elective-V Lab	40	--	--	40
	Total				**660**

& Phase-I: 40 Phase-II: 40

SUMMER TERM: For Category '1': B.E. Electronics Engineering (SEM VIII)					
Course Code	**Course Name**	**Marks**			
		ISE	**MSE**	**ESE**	**Total**
HSS81	Technology Entrepreneurship Lab	40	--	--	40
OE^	Open Elective @	40	10	20	70
OE^	Open Elective @	40	10	20	70
ELP81	Category-'1': Major Project-I	80**&**	--	20	100
MOOC	MOOC (Min 8 week course)	--	--	--	100
ABL5	Financial Planning, Taxation Policies and Investment (Noncredit)	--	--	--	--
INT	Internship	--	--	--	*****280
	Total				**660**

*** Kindly refer internship evaluation guidelines for 280 marks**

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Monitoring & Evaluation of Internship

Course Name: Internship Course Code: INT	MSE	ESE	Total Marks	Total Credits
Institute Supervisor Evaluation	70	70	140	05
Industry Mentor Evaluation	70	70	140	05
	140	140	280	10

For MSE and ESE: **60 Marks Rubrics Based Evaluation**
10 Marks Internship Report Evaluation

Parameters for Rubrics Based Evaluation of Intern

(Needs improvement=1; Satisfactory=2; Good=3; Excellent=4)

S.N.	Parameters	Scale (1 to 4)
1	Behaviors	
2	Performs in a dependable manner	
3	Cooperates with co-workers and supervisors	
4	Shows interest in work Learns quickly	
5	Shows initiative	
6	Accepts responsibility	
7	Accepts criticism	
8	Demonstrates organizational skills	
9	Shows good judgment	
10	Analyzes problems effectively	
11	Is self-reliant	
12	Communicates well	
13	Has a professional attitude and appearance	
14	Is punctual	
15	Uses time effectively	
Rate the following parameters for Internship Report (Needs improvement=1; Satisfactory=1.5; Good=2; Excellent=2.5)		
17	Writes effectively	
18	Uses technical knowledge and expertise	
19	Demonstrates creativity/originality	
20	Produces high quality work	
	Total (Out of 70)	

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE71A	IC and MEMS Technology	3	--	--	3	--	--	3
		Examination Scheme						
		ISE		MSE		ESE		Total
		20		20		60		100

Pre-requisite Course Codes		EL31: Analog Electronics-I EL33:Digital Circuits EL51: Linear Integrated Circuits EL61: VLSI Design
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Discuss integrated circuit fabrication processes
	CO2	Illustrate the sequence of process of semiconductor device fabrication
	CO3	Discuss fundamental principles of MEMS devices including physical operation and mathematical modeling.
	CO4	Apply various fabrication processes and materials for MEMS device fabrication and its Characterization with proper justification.
	CO5	Develop different concepts of micro system sensors and actuators for real world applications.

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Environment and Crystal Growth for VLSI Technology**		08
	1.1	**Environment**: Semiconductor technology trend, Clean rooms, Wafer cleaning.	1,2,3,4	
	1.2	**Semiconductor Substrate:** Phase diagram and solid solubility, Crystal structure, Crystal defects, Czochralski growth, Bridgman growth of GaAs, Float Zone growth, Wafer Preparation and specifications.	1,2,3,4	
2		**Fabrication Processes Part 1**		08
	2.1	**Deposition:** Evaporation, Sputtering and Chemical Vapor Deposition.	1,2,3,4	
	2.2	**Epitaxy:** Molecular Beam Epitaxy, Vapor Phase Epitaxy, Liquid Phase Epitaxy, Evaluation of epitaxial layers	1,2,3,4	
	2.3	**Silicon Oxidation:** Thermal oxidation process, Kinetics of growth, Properties of Silicon Dioxide, Oxide Quality, high κ and low κ dielectrics.	1,2,3,4	
	2.4	**Diffusion:** Nature of diffusion, Diffusion in a concentration gradient, diffusion equation, impurity behavior, diffusion systems, problems in diffusion, evaluation of diffused layers.	1,2,3,4	

	2,5	**Ion Implantation**: Penetration range, ion implantation systems, process considerations, implantation damage and annealing.	1,2,3,4	
3		**Fabrication Processess Part 2**		**08**
	3.1	**Etching:** Wet chemical etching, dry physical etching, dry chemical	1,2,3,4	
	3.2	**Lithography:**Photoreactive materials, Pattern generation and mask making, pattern transfer, Electron beam, Ion beam and X-ray lithography.	1,2,3,4	
	3.3	Device Isolation, Contacts and Metallization: Junction and oxide isolation, LOCOS, trench isolation, Schottky contacts, Ohmic contacts, Metallization and Packaging: Integrated circuit packages, Electronics package reliability	1,2,3,4	
	3.4	**CMOS Process Flow:** N well, P-well and Twin tub	1,2,3,4	
	3.5	Design rules, Layout of MOS based circuits (gates and combinational logic), Buried and Butting Contact.	1,2,3,4	
4		**Introduction to MEMS, MEMS Materials and Properties**		**10**
	4.1	Introduction to MEMS Technology, Difference between ICT & MEMS Technology, Difference between ICs and MEMS Devices and Real world Sensors/Actuators examples with brief description.	5, 7, 8, 9	
	4.2	Architecture, working and basic quantitative behaviour of MEMS devices like Cantilevers, Microheaters, Accelerometers, Pressure Sensors, Micromirrors in DMD, Inkjet printer-head.	5, 6, 7, 8	
	4.2	Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson's ratio, density, piezoresistive coefficients, TCR, Thermal Conductivity, Material Structure.	5, 7, 8	
	4.3	Bulk, Surface & LIGA Micromachining, Die, Wire & Wafer Bonding, Dicing, Packaging, MEMS Reliability.	8	
5		**MEMS Devices Fabrication and Characterization**		**06**
	5.1	Understanding steps involved and materials used in Fabricating MEMS device like Cantilevers, Microheaters, Accelerometers, Pressure Sensors, Micromirrors in DMD, Inkjet printer-head and Selection of Fab processes and materials based on fabrication of a given MEMS device and its intended application.	5, 7, 8	
	5.2	**MEMS Devices Characterization:** MEMS Device dimensions, Piezoresistance, TCR, Stiffness, Adhesion, Vibration, Resonant frequency, & importance of these measurements in studying device behavior.	8	**02**
			Total	**42**

ISE Evaluation:

1) Two Assignments based on (CO1-CO2-Assignment 1) & (CO3-CO4-Assignment 2). (5 Marks)
2) Case Study of MEMS device fabrication and characterization: Group Activity within Laboratory Batch [Evaluation during laboratory session. CO5. (10 Marks)]
3) Two Quiz based (CO1-CO2-Quiz 1) & (CO3-CO4-Quiz 2). (5 Marks)

Recommended Books:

[1] James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology", Pearson, Indian Edition.

[2] Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, Second Edition.

[3] Sorab K. Gandhi, "VLSI Fabrication Principles", Wiley, Student Edition.

[4] G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, First Edition.

[5] N. Maluf, K Williams,"An Introduction to Microelectromechanical Systems Engineering" Artech House Inc, Second Edition.

[6] Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing

[7] Microsystem Design - by S. Senturia; Publisher: Springer

[8] Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press

[9] Fundamentals of Microfabrication - by M. Madou; Publisher: CRC Press; Second edition

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE71B	Digital Signal Processing	3	--	--	3	--	-	3
		Examination Scheme						
		ISE		MSE	ESE		Total	
		20		20	60		100	

Pre-requisite Course Codes	EL-53 : Signal & System ELL-53 : Signals and Systems Lab ELL-64 : Signal Processing Lab	
After successful completion of the course, student will be able to,		
Course Outcomes	CO1	design digital IIR filter
	CO2	design digital FIR filter
	C03	analyze multi rate signal processing system
	CO4	apply LMS algorithm for adaptive filtering
	CO5	develop digital signal processing application

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1	**Digital IIR Filter**	1,2,4	12
	1.1	Introduction to Digital FiltersDigital IIR filter design using BLT Method, Digital Butterworth LPF & HPF design		
	1.2	Digital IIR filter design using Impulse Invariant Method(IIM) BLT Method		
	1.3	Digital IIR filter design using Bilinear Transformation Method (BLT)		
	1.4	Digital Butterworth filters		
	15	Lattice Realization structure		
2	2	**Digital FIR Filter**	1,2,4	12
	2.1	Linear Phase Concept , Position of definite ZEROS		
	2.2	Linear Phase FIR filter design using Windowing Method		
	2.3	Linear Phase realization		
	2.4	FIR filter design using frequency sampling method		
	2.5	Frequency sampling realization		
	2.6	Lattice Realization structure		
3	3	**Multi Rate Signal Processing**	4	8
	3.1	Sampling rate reduction: decimation by integer factors		
	3.2	Sampling rate increase: interpolation by integer factors		
	3.3	Sampling rate conversion by non integer factors		
	3.4	Multistage approach to sampling rate conversion		
	3.5	Polyphase decomposition		

4	**4**	**Adaptive Signal Processing**	5	6
	4.1	Concept Of Adaptive Filter		
	4.2	Minimum MSE Criterion, LMS Algorithms		
	4.3	Weiner Filter, Steepest descent search and the LMS algorithm.		
	4.4	Kalman filter		
5	**5**	**Applications of DSP**	1,3	6
	5.1	Subband coding		
	5.2	Channel Equalization, Active Noise Control Echo Cancellation		
	5.3	Signal Compression		
		Total		**42**

Recommended Books:

[1] S.Salivahanan, AVallavaraj, C Gnanapriya, "Digital Signal Processing", Tata McGraw Hill, First Edition.

[2] John Proakis and DimitrisMonolakis, "Digital Signal Processing", Pearson Publication, Forth Edition.

[3] Alan V. Oppenheim, Alan S. Willsky, and S. Hamid Nawab, "Signals and Systems", Second Edition, PHI learning.

[4] P. RameshBabu, "Digital Signal Processing", ScitechPublication Pvt. Ltd. 4th edition.

[5] Emmanuel Ifeachor and Barrie Jervis, "Digital Signal Processing : A Practical Approach", 2nd Edition, Pearson Education Limited

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		L	T	P	L	T	P	Total
ELE72A	Analog CMOS VLSI Design	3	--	--	3	--	-	3
		Examination Scheme						
		ISE		MSE	ESE		Total	
		20		20	60		100	

Pre-requisite Course Codes		ES11: Basic Electrical & Electronics Engineering EL31: Analog Electronics-I EL32: Digital Circuits EL41: Analog Electronics-II EL51: Linear Integrated Circuits EL61: VLSI Design
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Recognize trade-offs involved in analog VLSI Circuits
	CO2	Analyze current mirrors and bandgap references as basic building blocks of CMOS analog VLSI circuits
	CO3	Analyze given amplifier using small signal model as well as large signal methodology
	CO4	Derive and interpret frequency response and noise behaviour of amplifiers
	CO5	Describe layout techniques for analog circuits
	CO6	Design MOSFET based operational amplifiers for VLSI circuits

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**CMOS analog building blocks**		10
	1.1	**MOS Models:** Necessity of CMOS analog design, Review of characteristics of MOS device, MOS small signal model, MOS spice models	1, 2	
	1.2	**Passive and Active Current Mirrors:** Basic current mirrors, Cascode current mirrors and Active current mirrors	1, 2	
	1.3	**Band Gap References:** General Considerations, Supply-independent biasing, Temperature independent references, PTAT current generation and Constant Gm biasing	1, 2	
2		**Single Stage Amplifiers and Differential Amplifiers**		10
	2.1	**Single Stage Amplifiers:** Basic concepts, Common source stage (resistive load, diode-connected load, current-source load, triode load and source degeneration), Source follower, Common gate stage, Cascode stage	1	
	2.2	**Differential Stage Amplifiers:** Single ended and differential operation, Basic differential pair, Common-mode response, Differential pair with MOS loads, Gilbert cell	1	

3		**Frequency Response, Noise and Analog Layout**		10
	3.1	**Frequency Response:** General considerations, Common-source stage, Source followers, Common-gate stage, Cascode stage and Differential pair.	1	
	3.2	**Noise**: Statistical Characteristics of noise, types of noise, representation of noise in circuits, noise in single stage amplifiers and differential pair.	1	
	3.3	**Analog Layout Techniques:** Antenna effect, Resistor matching, capacitor matching, current mirror matching, floorplanning, shielding and guard rings	1,2, 4	
4		**MOS Operational Amplifiers**		6
	4.1	**Op-amp:** General Considerations, performance parameters, One-stage op-amps, Two-stage op-amps, Gain Boosting, Common-mode feedback, Input range limitations, Slew Rate, Power supply rejection, Noise in op-amps.	1	
	4.2	**Stability and Frequency Compensation:** General Considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps.	1	
5		**Design of Amplifiers**		6
	5.1	Design of Differential amplifiers. Design of two stage op-amps.	3, 4	
			Total	**42**

Recommended Books:

[1] B Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 1st Edition.

[2] R. Jacaob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, Student Edition

[3] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition.

[4] Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", Willey, 5th Edition

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE72B	Image Processing & Applications	3	--	--	3	--	-	3
		Examination Scheme						
		ISE		MSE	ESE		Total	
		20		20	60		100	

Pre-requisite Course Codes		BS31: Applied Mathematics I BS41: Applied Mathematics II EL-53 : Signal & System
After successful completion of the course, student will be able to		
Course Outcomes	CO1	apply Image enhancement technique
	CO2	apply image segmentation and binary image processing technique
	CO3	interpret 2D signals in transform domain
	CO4	solve image compression and decompression techniques
	CO5	apply quantitative models of image and video processing for various engineering applications

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Image Fundamentals & Enhancement**		**12**
	1.1	Image acquisition, Sampling and Quantization, Basic Relationship Between Pixels.	1,2	
	1.2	Spatial Domain Point Processing: Digital Negative, Contrast Stretching, Thresholding, Gray Level Slicing, Bit Plane Slicing, LOG Transform and Power Law Transform.	1,2	
	1.3	Neighborhood Processing: Averaging filters, Order Statistics Filters, High Pass Filters and High Boost Filters	1,2	
	1.4	Frequency Domain Processing: DFT for filtering and Homomorphic filters.	1,2	
	1.5	Histogram Modeling: Histogram Equalization and Histogram Specification.	1,2	
2		**Two Dimensional Transforms**		**8**
	2.1	Discrete Fourier Transform, Properties of DFT and Fast Fourier Transform	1,2,3	
	2.2	Discrete Cosine Transform	1,2,4	
	2.3	Discrete Hadamard Transform, Fast Hadamard Transform Algorithm,	1,3	

	2.4	Discrete Wavelet Transform	4	
3		**Image Segmentation and Morphology**		**10**
	3.1	Point, Line and Edge Detection, Edge Linking using Hough Transform and Graph Theoretic Approach, Thresholding, and Region based Segmentation.	1,2,4	
	3.2	Dilation, Erosion, Opening, Closing, Hit or Miss Transform, Thinning and Thickening, and Boundary Extraction on Binary images	1,2,4	
4		**Image Compression**		**6**
	4.1	Introduction, Redundancy, Fidelity Criteria	1,2	
	4.2	Lossless Compression Techniques : Run Length Coding, Arithmetic Coding, Huffman Coding, Differential PCM	1,2	
	4.3	Lossy Compression Techniques: Improved Gray Scale Quantization, JPEG baseline System, MPEG-1	1,2	
5		**Applications of Image Processing**		**6**
	5.1	Digital Watermarking, Biometric Authentication (Face, Finger Print, Signature Recognition), Vehicle Number Plate Detection and Recognition, Object Detection using Correlation Principle, Handwritten and Printed Character Recognition, Contend Based Image Retrieval, Text Compression.	4,5	
			Total	**42**

Recommended Books:

[1] S. Jayaraman, E.Esakkirajan and T.Veerkumar, "Digital Image Processing" TataMcGraw Hill Education Private Ltd, 2009.

[2] Rafel C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education Asia, Third Edition, 2009.

[3] Anil K. Jain, "Fundamentals and Digital Image Processing",Prentice Hall of India Private Ltd, Third Edition.

[4] S. Sridhar, "Digital Image Processing',Oxford University Press, Second Edition, 2012.

[5] Robert Haralick and Linda Shapiro, "Computer and Robot Vision", Vol I, II, Addison Wesley, 1993.

Sardar Patel Institute of Technology

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE73A	Photovoltaic systems and Smart Grid	3	---	--	3	--	--	3
		Examination Scheme						
		ISE		MSE	ESE			Total
		20		20	60			100

Pre-requisite Course Codes		ES11: Basic Electrical & Electronics Engineering EL42: Principles of Control Systems EL62: Power Electronics
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Compare different available renewable energy resources
	CO2	Evaluate parameters of PV modules in different interconnecting modes.
	CO3	Analyze PV power system to optimize it's performance parameters.
	CO4	Discriminate Smart Grid Architecture and Design.

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Introduction to renewable energy sources**		06
	1.1	Renewable and non-renewable energy sources, solar radiation energy, Estimating energy requirement, Energy from solar PV conversion, other renewable energy technologies	1,2,3	
	1.2	Solar cells, PV cell characteristics and equivalent circuit, Model of PV cell, Short circuit, Open circuit and Peak power parameters, Factors affecting electricity generated by solar cell, Cell efficiency, Fill factor	1,2,3	
2		**Interconnection and Sizing of PV module**		12
	2.1	Identical cells in series, Load line, Non Identical Cells in series, Protecting cells in series, Interconnecting modules in parallel, Identical cells in parallel, Load line in parallel, Non Identical Cells in parallel, Protecting cells in parallel	1,2,3	
	2.2	Sizing PV for applications without batteries, Battery Batteries, Battery Energy and Power Densities, Battery Selection, Battery Comparison, Other Energy storage methods, Battery Charger, Charge controller, PV system design	1,2,3	
3		**Maximum Power Point Tracking**		06
	3.1	MPPT concept, Input impedance of Buck Converter, Input impedance of Boost Converter, Input impedance of Buck and Boost Converter	1,2,3	
	3.2	MPPT Algorithm: Impedance control method, Reference cell voltage scaling method, Reference cell current scaling method	1,2,3	

	3.3	Power slope method, Gate Driver, MPPT for Non resistive method,	1,2,3	
4		**Smart Grid Architecture, Communications and Measurement Technology**		**08**
	4.1	Today's grid versus smart grid, Standards for smart grid system, Functions of smart grid,	3,4,5	
	4.2	Communication and Measurement, Monitoring PMU, Smart Meters and Measurements Technologies, GIS and Google Mapping tool, Multiagent System Technologies, Microgrid and smart grid comparison	3,4,5	
5		**Computational Tools for Smart Grid Design**		**10**
	5.1	Introduction to smart computational tools, Decision Support Tools (DS), Optimization Techniques, Classical Optimization Methods, Heuristic Optimization,	3,4,5	
	5.2	Evolutionary Computational Techniques, Adaptive Dynamic Programming Techniques, Pareto Methods, Hybridizing Optimization Techniques and Applications to the Smart Grid	3,4,5	
			Total	**42**

ISE Evaluation:

Case studies from three different locations in Mumbai 10M
Two quizzes 5M (Best of the two)
Two Assignments (Average of Two)

Recommended Books:

1. Chetan Solanki, "Solar Photovoltaics: Fundamentals, Technologies And Applications, PHI Publication, 3rd Edition.
2. Alexander P. Kirk, "Solar Photovoltaic Cells", Academic Press.
3. Qing-Chang Zhong, Tomas Hornik, "Control of Power Inverters in Renewable Energy and Smart Grid Integration", Wiley Publications, IEEE press.
4. Janaka B. Ekanayake, Nick Jenkins, KithsiriLiyanage, Jianzhong Wu, Akihiko Yokoyama, "Smart Grid: Technology and Applications" Wiley Publications.
5. James Momoh, "Smart Grid Fundamentals of Design and Analysis", Wiley Publications, IEEE press.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE 73B	Computer and Communication Networks	03	--	--	03	--	--	03
		Examination Scheme						
		ISE		MSE		ESE		Total
		20		20		60		100

Pre-requisite Course Codes		EL44: Fundamentals of Communication Engineering EL63:Digital Communication
Course Outcomes	At the end of the successful completion of the course students will be able to	
	CO1	Recognize the significance of OSI and TCP IP models in networking
	CO2	Choose relevent techniques, algorithms and protocols used by OSI layers
	CO3	Solve network issues by using IP addressing concepts.
	CO4	Identify various network security threats

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1.1	Topologies, LAN, MAN, WAN, Wireless network	1,2	06
	1.2	Reference Models: Layers details of OSI, TCP/IP Models		
	1.3	Introduction to physical media such as cables,router, switch		
2	2.1	Aloha protocols, Carrier Sense Multiple Access (CSMA) and multiplexing techniques assocaited with physical layer	1,2	05
	2.2	Congestion and flow control mechanisms associated with transport and data link layers: Fairness algorithms, Stop and Wait protocols.		06
	2.3	Application layer protocols such as HTTP, FTP, SMTP, DNS, peer to peer file sharing protocol.		06
3	3.1	IP addressing schemes, Subnet masks, Subnetting and Supernetting with examples of class A, B and C.	1,2	06
4	4.1	Introduction to information security, Challenges of Securing Information.	3,4	02
	4.2	Cryptography, Enterprise Network Security: DMZ, NAT, SNAT, DNAT, Port Forwarding.		06
	4.3	**Attacks**:Denial of Service (DoS), SQL injection, replay, botnets.		02
	4.4	**Cyber crime and Cyber forensics**		03
			Total	42

Recommended Books:

[1] Behrouz A Forouzan, Data communications and Networking , McGraw-Hill Publication, Forth Edition.

[2] William Stallings, Data Computer Communications, Pearson Education.

[3] Information Security by Mark Stamp and Deven Shah by Wiley Publications.

[4] CompTIA ® Security+ Guide to Network Security Fundamentals, Fifth Edition by Mark Ciampa.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL71A	IC and MEMS Technology Lab	--	--	02	--	--	1	1
		Examination Scheme						
		ISE		MSE	ESE		Total	
		40		--	--		40	

Pre-requisite Course Codes		EL31: Analog Electronics-I EL33:Digital Circuits EL61: VLSI Design ELE71A: IC and MEMS Technology
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Make use of modern/open source tools available for process simulation.
	CO2	Draw layout as per the design rules and simulate the characteristics of a given MOS circuit to arrive at valid conclusion using Industry graded VLSI CAD tools.
	CO3	Design and simulate MEMS devices and system using Industry graded MEMS FEA CAD/simulation tools like COMSOL and Coventorware.
	CO4	Design and simulate MEMS devices and system using open source simulation tools like sugar.
	CO5	Determine characteristics of given MEMS device using Hardware setup.

Exp. No.	Experiment Details	Ref.	Marks
1	**Aim:** Use nanohub platform to simulate and analyze the Oxidation process for various process parameters and wafer specifications. **Problem Statement:** Simulate the oxidation process with Deal - Groove model for different conditions (eg. Oxidation type, orientation, time, temperature, thickness etc.) and comment on the results obtained.	1,2	**05**
2	**Aim:** Use nanohub platform to simulate and analyze the diffusion process for various given conditions. **Problem Statement:** Simulate the diffusion process for various given conditions. Such as eg. Source, time, temperature, dopant etc. and comment on the results obtained.	1,2	**05**

3	**Aim:** To use Industry graded VLSI CAD tools to draw layout and analyze CMOS Inverter circuit. **Problem Statement:** Draw and simulate CMOS Inverter. Carry out static as well as transient simulation. Analyze CMOS Inverter for i) $(W/L)_{PMOS} > (W/L)_{NMOS}$ ii) $(W/L)_{PMOS} = (W/L)_{NMOS}$ iii) $(W/L)_{PMOS} < (W/L)_{NMOS}$. Do parasitic extraction. Feed these parasitic in circuit simulator and do the layout versus schematic verification.	3,4	**05**
4	**Aim:** To use Industry graded VLSI CAD tools to draw layout and analyze MOS based circuit. **Problem Statement:** a. Draw and simulate layout for the following circuits. Size them with respect to reference inverter A: CMOS NAND B: CMOS NOR b. Draw and simulate layout for 6T SRAM cell for high reliability and lowest area. c. Draw and simulate layout for given flipflop (SR, D, T, JK). d. Draw and simulate layout for half adder. e. Draw and simulate layout for logic equation using Static CMOS, dynamic logic, transmission gate. **(Any one problem statement for a group of student)**	3,4	**05**
5	**Aim:** To analyze MEMS cantilever in Matlab. **Problem Statement:** For the given MEMS cantilever with given dimensions and uniformly distributed load i. To plot the variation in stiffness constant (K) for varying length (L) keeping its width (W), thickness (h) constant and different values of effective length ($\lambda r = L/Lc$) of uniformly distributed load. ii. To plot the variation in stiffness constant (K) for varying width (W) keeping its length (L), thickness (h) constant and different values of effective length ($\lambda r = L/Lc$) of uniformly distributed load. iii. To plot the variation in stiffness constant (K) for varying thickness (h) keeping its width (W), length (L) constant and different values of effective length ($\lambda r = L/Lc$) of uniformly distributed load.	5	

6	a. **Aim:** To model and analyze MEMS cantilever in COMSOL Multiphysics. **Problem Statement:** i. For the given dimensions and material create MEMS cantilever model in COMSOL and observe the dependence of resonance frequency of the cantilever on material. ii. For the cantilever model analyze dependence of fundamental resonance frequency on varying length (given range), plot the result and also compare the result with analytical expression of resonance frequency. b. **Aim:** To model and analyze the Hot Arm actuator in COMSOL Multiphysiscs. **Problem Statement:** For the given model of Hot Arm actuator in COMSOL Multiphysiscs, i. Describe the complete process flow, schematic representation of the mask layout and draw the final structure. ii. Observe the spatial variation of electric potential, temperature of the Hot Arm actuator before and after the deflection of the Hot Arm actuator. iii. Observe and draw the effect of change in width of flexures on the deflection of the Hot Arm actuator. c. **Aim:** To model and analyze Piezoresitive Pressure Sensor in MEMS Design and Simulation FEM Tool (CoventorWare). **Problem Statement:** i. Choose the proper substrate; define the process flow and Layout of Piezoresitive pressure sensor in MEMS Design and Simulation FEM Tool (CoventorWare) and create a its 3- D Layout. ii. Observe the change in resistance of piezoresistance for given input pressure. Compare this reading with the given analytical expression of the change in resistance of the piezoresistace. **(Any one problem statement for a group of student either using COMSOL OR CoventorWare)**	5,6,7	**05**
7	a. **Aim:** To analyze MEMS Piezoelectric Harvester model in Sugar tool. **Problem Statement:** Choose the proper configuration, dimensions and the method of conversion (converter) for obtaining dc voltage from ac voltage generated by the MEMS Piezoelectric Harvester. Obtain the output voltage graph for any two different substrates materials against Silicon as a substrate material. b. **Aim:** To analyze MEMS cantilever in Sugar Tool. **Problem Statement:**	1, 5	**05**

	Choose the proper dimensions of MEMS cantilever modeled in Sugar. Choose the proper co-ordinate and node for applied point contact force. Observe and tabulate the maximum displacement of the cantilever for at least three different values of point contact load, verify one of the readings with given analytical expression of maximum displacement of the cantilever. **(Any one problem statement for a group of student)**		
8	**Aim:** To evaluate the performance of the fabricated MEMS microheater. **Problem Statement:** For the given fabricated MEMS micro-heater, i. Measure the temperature of the heated membrane for the input ii. Plot the temperature response of heated membrane to standard test voltages like square, Ramp, and sinusoidal.	5	**05**
		Total	**40**

References:

[1] www.nanohub.org

[2] James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology", Pearson, Indian Edition

[3] Eugene D. Fabricius, "Introduction to Very Large Scale Integration Design", McGraw-Hill, 1990 - Technology & Engineering -Indian Edition

[4] Microwind User Manual

[5] MEMS Technology Laboratory Manual

[6] Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing

[7] Microsystem Design - by S. Senturia; Publisher: Springer

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL71B	Digital Signal Processing Lab	--	--	02	--	--	01	01
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes	EL-53 : Signal & System ELL-53 : Signals and Systems Lab ELL-64 : Signal Processing Lab	
Course Outcomes	After successful completion of the course, student will be able to,	
	CO1	design and Implement Digital IIR filter
	CO2	design and implement Digital FIR filter
	C03	perform upsampling and downsampling of signal
	CO4	develop application of DSP

Expt. No.	Topics	Ref.	Marks
1	Digital Butterworth Filter Design using Impulse Invariant Method	1,2,3,4	5
2	Digital Butterworth Filter Design using BLT Method	1,2,3,4	5
3	Linear Phase FIR Filter Design using Windowing Method	1,2,3,4	5
4	Linear Phase FIR Filter Design using Frequency Sampling Method	1,2,3,4	5
5	Multirate Signal Processing	4	5
6	Adaptive Filtering	5	5
7	Mini Project on real Time DSP application	5,6	10
	Total Marks		40

References :

[1] S.Salivahanan, AVallavaraj, C Gnanapriya, "Digital Signal Processing", Tata McGraw Hill, First Edition.

[2] John Proakis and DimitrisMonolakis, "Digital Signal Processing", Pearson Publication, Forth Edition.

[3] Alan V. Oppenheim, Alan S. Willsky, and S. Hamid Nawab, "Signals and Systems", Second Edition, PHI learning.

[4] P. RameshBabu,"Digital Signal Processing", ScitechPublication Pvt. Ltd. 4th edition.

[5] Emmanuel Ifeachor and Barrie Jervis, "Digital Signal Processing : A Practical Approach", 2nd Edition, Pearson Education Limited

[6] Vinay K. Ingle , John G. Proakis, "Digital Signal Processing Using MATLAB",Cengage Learning

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL72A	Analog CMOS VLSI Design Lab	--	--	2	--	--	2	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		ELL61: VLSI Design Lab
After successful completion of the course, student will be able to		
Course Outcomes	CO1	verify characteristics of MOSFET based analog circuits via simulations
	CO2	analyze and discuss tradeoffs in CMOS analog circuits after successful simulations
	CO3	use the features of Cadence tool efficiently and effectively to solve the given task
	CO4	create scientific document for the experiments carried out
	CO5	demonstrate the desire for learning by carrying out activity for the content beyond syllabus in the VLSI analog domain

Exp No.	Experiment Details	Ref.	Marks
1.	Simulation to obtain and tabulate analog parameters of NMOS and PMOS devices	1,2,3	5
2.	Design and Simulation of Current Mirrors and/or Bandgap References	1,2,3	5
3.	Design and Simulation of Various Configurations of Common Source Single Stage Amplifier	1,2,3	5
4.	Design and Simulation of Common Drain and Common Gate Single Stage Amplifier	1,2,3	5
5.	Design and Simulation of Two Stage Operational Amplifier	2,3,4	5
6.	Layout Simulation of Operational Amplifier	2,3,4	5
7.	Simulate the circuit in the given IEEE paper	5	10
	Total		40

Recommended Books:

1. B Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 1st Edition.
2. R. Jacaob Baker, Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, Student Edition
3. P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition.
4. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog Integrated Circuits", Willey, 5th Edition
5. IEEE Transaction Papers

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL72B	Image Processing & Applications Lab	--	--	2	--	--	2	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		
After successful completion of the course, student will be able to		
Course Outcomes	CO1	apply Image enhancement technique on image.
	CO2	apply image segmentation technique on image.
	CO3	applymorphological operators on binary image.
	CO4	applylossy and lossless compression techniques.
	CO5	develop video based applications

Exp No.	Experiment Details	Ref.	Marks
1.	Image Enhancement	1 to 5	5
2.	Image Segmentation	1 to 5	5
3.	Image Morphology	1 to 5	5
4.	Image Compression	1 to 5	5
5.	Mini Project: Real time video applications	Published Research Paper	20
	Total		40

Recommended Books:

[1] S. Jayaraman, E.Esakkirajan and T.Veerkumar, "Digital Image Processing" TataMcGraw Hill Education Private Ltd, 2009.
[2] Rafel C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson Education Asia, Third Edition, 2009.
[3] Anil K. Jain, "Fundamentals and Digital Image Processing", Prentice Hall of India Private Ltd, Third Edition.
[4] S. Sridhar, "Digital Image Processing", Oxford University Press, Second Edition, 2012.
[5] Robert Haralick and Linda Shapiro, "Computer and Robot Vision", Vol I, II, Addison Wesley, 1993.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL73A	Photovoltaic Systems and Smart Grid Lab	--	--	02	--	--	01	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		ES11: Basic Electrical & Electronics Engineering EL42: Principles of Control Systems EL62: Power Electronics
At the end of the course students will be able to		
Course Outcomes	CO1	Obtain the characteristics of PV modules for the different interconnections using simulation software.
	CO2	Estimate the energy requirement and design a PV system for the required specifications of load.
	CO3	Develop an MPPT algorithms using PSIM simulation.

Sr. No.	Topics	CO	Marks
1	Install the gEDA and simulate the characteristics of PV cell using gEDA simulation software. Observe the change for different resistive load.	1	05
2	Simulate the characteristics of PV cell connected in series and connected in parallel using NGSPICE.	1	05
3	Estimate the daily energy requirement of the given location and based on that estimate the monthly energy requirement, and also estimate the monthly electricity bill according to the per unit kWh cost.	2	05
4	Obtain the characteristics of the given PV panel by putting its characteristics parameters in the PSIM simulation software. Verify at least four reading from the actual reading.	3	05
5	Obtain the I-V, P-V characteristics at T=25 degree C, irradiance=1000W/m2, after calculation of Rs and Rp using PSIM. Also obtain the characteristics for different irradiance.	1	05
6	Obtain the I-V, P-V characteristics at T=25 degree C, irradiance=1000W/m2, after calculation of Rs and Rp using PSIM. Also obtain the characteristics for different temperature.	1	05
7	Obtain the P-V characteristics of three series connected PV panels at T=25 degree C for different irradiance=1000W/m2 and 500W/m2, by MATLAB simulink. Y axis power and X axis Voltage. Obtain the shadow effect.	1	05

8	Design P & O algorithm using PSIM and observe the change also obtain the simulation of the Buck Converter with MPPT controller by using PSIM software.	3	05
	Total		40

Recommended Books:

1. Chetan Solanki, "Solar Photovoltaic Technology and Systems: A Manual for Technicians, Trainers and Engineers, PHI Publication
2. SailendraNathBhadra, "Electric Machinery Experiments: Laboratory Practices and Simulation Studies" Narosa Publication

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL73B	Computer and Communication Networks Lab	--	--	02	--	--	01	01
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		EL44: Fundamentals of Communication Engineering EL63:Digital Communication
Course Outcomes	At the end of the successful completion of the course students will be able to	
	CO1	Have an hands-on experience on networking cables & command line tools
	CO2	Do analytical studies of Computer Networks through network simulation tools/Scripting Languages
	CO3	Examine the current challenges in computer security and identify possible solutions to relsove the same.
	CO4	Adapt open source packet analyzers for communication networks

Sr. No.	Topics	Ref.	Marks
1	Identify and observe the behaviour of networking command line tools in Ubuntu/Windows OS environment.	1,2, 4	**5**
2	To build and test straight through UTP ethernet network cables.	1,2	**5**
3	Write a program in C to identify the IP address, Subnet mask, DNS server address and Hardware address of the client device.	1,2	**5**
4	Write a program in C/C++/Python to determine the administrators requirement to define the number of subnets, host/subnet, customized subnet masks and valid subnet ranges for a class C IP addressing scheme.	1,2	**5**
5	Examine Data Breaches and Scan for Malware Using the Microsoft Safety Scanner	3,4	**5**
6	Create a Virtual Machine of Windows 8/8.1 for Security Testing	3,4	**5**
7	Hands-on experience on how to Write-Protect and Disable a USBFlash Drive	3,4	**5**
8	Protocol Visualization with Packet Tracer.	5	**5**
	Total		**40**

References :

[1] Behrouz A Forouzan, Data communications and Networking , McGraw-Hill Publication, Forth Edition.

[2] William Stallings, Data Computer Communications, Pearson Education.

[3] Information Security by Mark Stamp and Deven Shah by Wiley Publications.

[4] CompTIA ® Security+ Guide to Network Security Fundamentals, Fifth Edition by Mark Ciampa.

[5] https://www.netacad.com/courses/packet-tracer

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE81A	Mixed Signal VLSI Design	3	--	--	3	--	-	3
		Examination Scheme						
		ISE		MSE	ESE		Total	
		20		20	60		100	

This course is intended to teach advance design techniques for comparators, ADC/DAC, oscillators and PLL. The course will give practical aspect of mixed signal VLSI blocks such ascomparators, data converters, oscillators and phase locked loop. As a part of this course, students will use industry standard software's and tools. The design problems given in the form of assignments will be designed andsimulated in a standard CMOS technology by students. The study will cover design issues like PVT variations. In summary, the course is designed with considering the need of VLSI design industry.

Pre-requisite Course Codes		ES11: Basic Electrical & Electronics Engineering EL31: Analog Electronics-I EL32: Digital Circuits EL41: Analog Electronics-II EL51: Linear Integrated Circuits EL61: VLSI Design ELE71A: Analog CMOS VLSI Design
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Apply the theory of MOSFET as a Switch to redesign opamp based circuits
	CO2	Apply the basic principles of oscillators and argue on various trade-offs arising in the design of Phase Lock Loop.
	CO3	Differentiate between various architectures of Analog to Digital Converters from the perspective of fundamentals of data converters
	CO4	Differentiate between various architectures of Digital to Analog Converters from the perspective of fundamentals of data converters

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Switched capacitor circuits and Comparators**		12
	1.1	**Switched capacitor circuits**: MOSFET as switches, Speed considerations, Precision Considerations, Charge injection cancellation, Unity gain buffer, Non-inverting amplifier and integrator.	1,3,4	
	1.2	**Comparators:** Comparator Specifications, Using an Op-amp for a Comparator, Charge-Injection Errors and Latched Comparators	2	
2		**Oscillators and Phase-Locked Loop**		10
	2.1	**Oscillators:** General considerations, Ring Oscillators, LC	1,3,4	

		Oscillators and VCO		
	2.2	**Phase-Locked Loop:** Simple PLL, Charge pump PLL, Nonideal effects in PLL, Delay Locked Loops and Applications of PLL in integrated circuits.	1,3,4	
3		**Nyquist-Rate D/A Converters**		10
	3.1	**Data Converter Fundamentals:** Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Signed Codes and Performance Limitations	2	
	3.2	**Nyquist-Rate D/A Converters**: Decoder-Based Converters, Binary-Scaled Converters, Thermometer-Code Converters and Hybrid Converters	2	
4		**Nyquist-Rate A/D Converters**		10
	4.1	Integrating Converters, Successive-Approximation Converters, Algorithmic (or Cyclic) A/D Converter, Pipelined A/D Converters, Pipeline A/D Converters, Flash Converters, Two-Step A/D Converters and Interpolating A/D Converters	2	
			Total	**42**

Recommended Books:

[1] B Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 1st Edition.

[2] Tony Chan Carusone, David A. Johns and Kenneth W.Martin "Analog Integrated Circuit Design", John Wiley and Sons, 2nd Edition

[3] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition.

[4] Gray, Meyer, Lewis, Hurst, "Analysis and Design of Analog Integrated Circuits", Willey, 5th Edition

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE81B	Neural Network and Fuzzy Systems	3	---	--	--	--	--	3
		Examination Scheme						
		ISE		MSE		ESE		Total
		20		20		60		100

Pre-requisite Course Codes		Knowledge of linear algebra, multivariate calculus, and probability theory. Knowledge of a programming language (MATLAB /C/C ++ , Python recommended)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Demonstrate the learning principle of neural networks.
	CO2	Construct neural network applications using supervised learning.
	CO3	Construct neural network applications using unsupervised learning.
	CO4	Apply fuzzy logic concepts to design fuzzy control System

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1	**Fundamentals of Artificial Neural Networks (ANN)**		**06**
		Fundamental concepts, Basic models, Important Terminologies, Mc-Cullotch-Pits Neuron, Linear Separability	1,2,3	
2		**Supervised Learning Networks**		**12**
	2.1	Introduction, Perceptron Networks, Adaptive Linear Neuron, Multiple Adaptive Neurons, Back Propagation Network	1,2,3	
3		**Unsupervised learning network**		**12**
	3.1	Introduction, Competitive Neural nets	1,2,3	
	3.2	Kohonen Self-Organizing Feature Maps, Learning Vector Quantization, Adaptive Resonance Theory	1,2,3	
4		**Concepts of Fuzzy logic and Fuzzy Control System**		**12**
	5.1	Introduction to Fuzzy logic, Fuzzy sets, Fuzzy Relations, Membership Functions	3,4,5	
	5.2	Fuzzification, Defuzzification, Fuzzy Inference System, Fuzzy logic control (FLC) systems, Applications of FLC. Neuro-Fuzzy Hybrid Systems	3,4,5	
Total				**42**

ISE Evaluation:

Case studies (02) 10M
Two quizzes 05 M (Best of the two)
Two Assignments 05 M (Average of Two)

Recommended Books:

1. Simon Haykin, "Neural Network a - Comprehensive Foundation", Pearson Education
2. S.N. Sivanandam, S.N. Deepa, "Introduction to Soft computing tools," Wiley Publication
3. Samir Roy, UditChakraborty , "Soft Computing, Neuro-Fuzzy and Genetic Algorithms," Pearson India Education.
4. Satish Kumar Neural Networks:A classroom Approach Tata McGraw-Hill
5. Thimothv J. Ross, "Fuzz V Logic with Engineering Applications", McGraw -Hill
6. Rajsekaran S, VijaylakshmiPai, Neural Networks, Fuzzy Logic, and Genetic Algorithms, PHI
7. Hagan, Demuth, Beale, "Neural Network Design," Thomson Learning
8. Christopher M Bishop, "Neural Networks For Pattern Recognition," Oxford Publication
9. William W Hsieh Machine Learning Methods in the Environmental Sciences Neural Network and Kernels, Cambridge Publication

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE81C	Electronic System Design	3	--	--	3	--	--	3
		Examination Scheme						
		ISE		MSE		ESE		Total
		20		20		60		100

Pre-requisite Course Codes	EL33 (Digital Circuits) EL43 (Computer Organization and Architecture) EL52 (Micro-Architectures) ELL63 (Fundamentals of Operating Systems Lab)	
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Get insight of design metrics of Embedded system to design real time applications to match recent trends in technology.
	CO2	Understand the Real time operating system concepts
	CO3	Know the Hardware-Software design issues and testing methodology of Embedded system
	CO4	Design reliable embedded system

Module No.	Unit No.	Topics	Ref.	Hrs.
1		**Fundamentals of Embedded System**		08
	1.1	Introduction to Embedded Systems, Characteristics of Embedded System, Design Process, Design Metrics and optimization of various parameters of embedded system. Real time System's requirements, real time issues, interrupt latency	1	
	1.2	Embedded Product development lifecycle, Program Modeling concepts: DFG, FSM, Petri-net, UML	1	
2		**Embedded Hardware and Design**		08
	2.1	Introduction to ARM-v7-M (Cortex-M3), ARM Architecture, Comparison of ARM-v7-A (Cortex A8), ARM-v7-R (CortexR4), ARM-v7-M (Cortex-M3)	2	
3		**Real time Operating System**		08
	3.1	Tasks, Task states, Message Queue, Mailbox, Pipe Function, Mutex, RPC Function, Shared Resources	1,3,4	
	3.2	Interprocess Communication, Semaphore, Spinlock Semaphore, round robin scheduler, Blocking Semaphore, Mailbox, Pre-emptive scheduler		
4		**Introduction to MicroC/OS-II: real time Kernel**		08
	4.1	Foreground Background System, Critical Section of codes, Task control Blocks, Task Scheduling, Creating a Task and Deleting a Task.	4	

	4.2	Creating and Deleting Semaphore, Creating and deleting Mutex, creating and Deleting Mailbox, Creating and deleting Message Queue.		
5		**Industry Standards**		10
	5.1	Introduction to IEC 61508 standard : Organizing and managing the life-cycle, Requirements involving the specification, Requirements for design and development, Integration and test, Operations and maintenance, Validation, Modifications, Acquired sub-systems, Organizing and managing the software engineering.	05,06	
	5.2	Introduction to IEC 60601 standard : Protection of radio services, Protection of the Public Mains network, Immunity, Electrostatic Discharge, Radiated RF electromagnetic fields, Electrical fast transients and bursts.	07	
	5.3	Introduction to IEC 26262 : Introduction of ISO/DIS 26262 (ISO 26262), Parts of ISO 26262, ASIL Levels, Product Development – System Level, Product Development Software Level, Fitting software tools into ISO 26262 process.	08	
	5.4	Reliable Embedded System : Single-program, real-time embedded systems, TT vs. ET architectures, Modeling system timing characteristics, basic tick lists, determining the required tick interval, short tasks, importance of task offsets, task sequence initialization, task jitter, response times, importance of WCET/BCET information, challenges with WCET/BCET measurements, TTC scheduler.	09	
			Total	**42**

Recommended Books:

[1] Embedded System: Architecture, Programming and Design, Rajkamal, Tata McGraw-Hill Education, 2011

[2] ARM System-on-Chip Architecture, Steve Furber

[3] Embedded System: Real time Operating Systems for the ARM Cortex^{TM}M3, Jonathan W. Valvano, Create Space Independent Publishing Platform, 2012

[4] MicroC/OS-II: The Real Time Kernal, Jean J. Labrosse, CRC press, 05 Feb 2002.

[5] David Smith , Functional Safety, A Straightforward Guide to applying IEC 61508 and Related Standards, Elsevier.

[6] IEC 61508: IEC standard for the functional safety for electrical, electronics and programmable electronics equipment

[7] IEC 60601: IEC standard on Medical Electric Equipment

[8] IEC 26262: IEC standard on Road vehicles

[9] The Engineering of Reliable systems: LPC1769 Edition, Pont M. J (2014), Published by Safetty Systems.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELE81D	Radiating Systems	3	--	--	3	--	-	3
		Examination Scheme						
		ISE		MSE	ESE		Total	
		20		20	60		100	

Pre-requisite Course Codes		EL53 Signals and Systems, EL54 Electromagnetic Engineering
Course Outcomes	CO1	Describe the radiation mechanism and parameters of antenna
	CO2	Describe various types of antennas
	CO3	Discuss microstrip and smart antennas
	CO4	Discuss fundamental principles of microwave engineering
	CO5	Discuss the fundamental principle, construction and working principle of optics and light wave

Module No.	Unit No.	Topics	Ref.	Hrs.
1	1.1	Types of Antennas, radiation mechanism, current distribution on a thin wire antenna and fundamental parameters.	1	8
	1.2	Infinitesimal dipole, small dipole and half wavelength dipole	1	
2	2.1	Yagi Uda Antenna, Monopole, Loop Antenna, Slot Antennas, Helical Antennas, Horn antennas and Parabolic Reflectors	1	8
	2.2	Broadside and Endfire array	2	
3	3.1	Microstrip antenna Introduction: Rectangular Patch, Circular Patch, Quality Factor, Bandwidth, and Efficiency, Input Impedance, Coupling, Circular Polarization, Arrays and Feed Networks, Corporate and Series Feeds, Reflect array.	1,5	10
	3.2	Smart antennas Introduction, Need of smart antenna system, Overview of smart antenna system, Types of smart antennas, Switched beam system, Adaptive system, Beam forming, Fixed weight beam forming: Maximum signal-to-interference ratio beam-former, Minimum mean square error. Adaptive beam forming: LMS algorithm, Sample matrix inversion method.	1,5	

4		Microwave Engineering		10
	4.1	General Solutions for TEM, TE and TM waves. Parallel plate waveguide, rectangular waveguide, circular waveguide, stripline, microstrip, wave velocities and dispersion.	3	
	4.2	Scattering Matrix, Two Cavity Klystron and Gunn Diode	3	
5		Optical Communication		6
	5.1	Elements of an optical fiber transmission link, block diagram, Ray theory transmission, total internal reflection, acceptance angle, numerical aperture and skew rays	4	
	5.2	Modes, linearly polarized modes, electromagnetic mode theory and propagation and types of fibers according to refractive index profile.	4	
			Total	**42**

Recommended Books:

1. C. A. Balanis, "Antenna Theory – Analysis and Design" ,John Wieley&Sons,Inc. 2nd Edition, 2007
2. R. E. Collin, Antennas and Radio Wave Propagation, McGraw-Hill., 1985.
3. D. M. Pozar, Microwave Engineering, John Wiley & Sons Publication, 2013.
4. Gerd Kaiser, "Optical Fiber Communication" , Mc-Graw Hill Publication , Singapore, 4th Edition, 2012
5. Tapan Sarkar, Michael Wicks, "Smart Antennas", John Wiley and sons , 2013.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL81A	Mixed Signal VLSI Design Lab	--	--	2	--	--	2	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		ELL61: VLSI Design Lab ELE72A: Analog CMOS VLSI Design ELEL72A: Analog CMOS VLSI Design Lab
After successful completion of the course, student will be able to		
Course Outcomes	CO1	analyze and discuss tradeoffs in Switch Capacitor and Comparator circuits after successful simulations
	CO2	analyze and discuss tradeoffs in Oscillators and Phase-Locked Loopcircuits after successful simulations
	CO3	analyze and discuss tradeoffs in A/D Converterscircuits after successful simulations
	CO4	analyze and discuss tradeoffs in D/A Converterscircuits after successful simulations
	CO5	demonstrate the desire for life-long learning by implementing the given task related to the advance concepts in the VLSI analog and mixed signal domain

Exp No.	Experiment Details	Ref.	Marks
1.	Simulations of Switch Capacitor and Comparator circuits	1 to 5	5
2.	Simulations of Oscillators and Phase-Locked Loop	1 to 5	5
3.	Simulations of A/D Converters	1 to 5	5
4.	Simulations of D/A Converters	1 to 5	5
5.	Mini Project: Simulate the circuit in the given IEEE paper	6	20
	Total		40

Recommended Books:

[1]B Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 1st Edition.
[2] Tony Chan Carusone, David A. Johns and Kenneth W.Martin "Analog Integrated Circuit Design", John Wiley and Sons, 2nd Edition
[3] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition.
[4] Gray, Meyer, Lewis, Hurst, "Analysis and Design of Analog Integrated Circuits", Willey, 5th Edition
[5] R. Jacaob Baker, "CMOS Mixed Signal Circuit Design", Wiley, Student Edition
[6] IEEE Transaction Papers

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL81B	Neural Network and Fuzzy Systems Lab	--	--	02	--	--	01	
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		
At the end of the course students will be able to		
Course Outcomes	CO1	Evaluate performance of Neural Networks for Supervised learning
	CO2	Apply Neural Network for un-supervised learning
	CO3	Construct a model of fuzzy control System

Sr. No.	Topics	Ref.	Marks
1	Application of single layer Perceptron neural Network	1,2	5
2	Application of Adaptive Linear neural network	1,2	5
3	Application of Multiple Adaptive Linear neural network	1,2	5
4	Application of Back-propagation neural Network	1,2	5
5	Evaluation of Kohonen's Self Organizing Map	1,2	5
6	Illustration of the Fuzzy Operations and Relations.	1,2	5
7	Demonstration of Fuzzy Control System	1,2	5
8	Simulation of ANFIS	1,2	5
	Total		40

Recommended Books:

1. S. N. Sivanandam, S. Sumathi, "Introduction to Neural Network using Matlab," Tata McGraw-Hill
2. N. P. Padhy, S. P. Simon, "Soft Computing with Matlab Programming," Oxford University Press.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL81C	Electronic System Design Lab	--	--	2	--	--	1	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		ELE82A (Electronic System Design)
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Understand how applications that incorporate a real-time kernel differ from foreground/ background, or super-loop, applications
	CO2	Understand process flow of porting OS on Microcontroller
	CO3	Understand Micrium OS Kernel's API
	CO4	Know how to utilize many of the services that Micrium OS Kernel provides
	CO5	Understanding interprocess communication in Real time operating System
	CO6	Understanding scheduling strategies in Real time operating system

Exp. No.	Experiment Details	Ref.	Marks
1	Porting Micrium OS on Cortex M3 architecture and understanding file hierarchy.	02,03	05
2	Initializing the Kernel, Create Task and Start the Task in Micrium OS	01	05
3	Implementing Micrium OS interrupt Handler.	01	05
4	Performing Micrium OS Kernel Scheduling. (Pre-emptive Scheduler)	01	05
5	Implementing various Kernel Services in Micrium OS	01	05
6	Implementing Semaphore in Micrium OS.	01	05
7	Performing Shared Resources Protection in Micrium OS.	01	05
8	Implementing Mutexes in Micrium OS. OR Implementing Message Queues in Message Queues.	01	05
		Total Marks	40

Recommended Books:

[1] MicroC/OS-II: The Real Time Kernal, Jean J. Labrosse, CRC ress, 05 Feb 2002.
[2] https://www.silabs.com/documents/public/training/wireless/micrium-os-kernel.pdf
[3] https://www.silabs.com/support/getting-started/micrium-os#series

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELEL81D	Radiating Systems Lab	--	--	2	--	--	2	1
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		EL53 Signals and Systems, EL54 Electromagnetic Engineering
After successful completion of the course, student will be able to		
Course Outcomes	CO1	Simulate the given antenna using HFSS tool
	CO2	Measure antenna parameters
	CO3	Carry out test to determine parameters of optical fiber

Exp No.	Experiment Details	Ref.	Marks
1.	Probe feed patch antenna designing in HFSS using constant values	1,2,3	5
2.	Probe feed patch antenna designing in HFSS using variable values	1,2,3	5
3.	Measurement of antenna parameters for a given antenna	1,2,3	5
4.	VNA calibration and component testing	1,2,3	5
5.	Obtain the characteristics Klystron and/or Gunn	2,3,4	5
6.	Measurement of Numerical Aperture of a given optical fiber	2,3,4	5
7.	Simulate the circuit in the given IEEE paper	5	10
	Total		40

Recommended Books:

1. C. A. Balanis, "Antenna Theory – Analysis and Design" ,John Wieley&Sons,Inc. 2nd Edition, 2007
2. HFSS Manual
3. Gerd Kaiser, "Optical Fiber Communication" , Mc-Graw Hill Publication , Singapore, 4th Edition, 2012
4. VNA Manual
5. David M Pozar, "Microwave Engineering" , John Wieley&Sons,Inc. Hobokenh,New Jersey, Fourth Edition, 2012.
6. IEEE Transaction Papers

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
HSS81	Technology Entrepreneurship Lab	--	--	02	--	--	01	01
		Examination Scheme						
		ISE		MSE		ESE		Total
		40		--		--		40

Pre-requisite Course Codes		
After successful completion of the course, student will be able to,		
Course Outcomes	CO1	Identify problems worth solving
	CO2	Craft value proposition
	C03	Prepare B-Plan
	CO4	Draft Patent
	CO5	Register virtual company

Expt. No.	Topics	Ref.	Marks
1	**Opportunity Discovery** 1.1 Self-discovery 1.2 Effectuation Principle 1.3 Identification of problem worth solving 1.4 Looking for solutions 1.5 Present the problem Assignment Submission : Effectuation case study	1	8
2	**Value Proposition Canvas and Business Model** 2.1 Craft your value proposition 2.2 Presentation of Value Proposition Canvas 2.3 Business Model and Lean Approach (Finance, Marketing, Operations) 2.4 Presentation of Lean Canvas Assignment Submission : Presentation of Value Proposition Canvas	2,3	8
3	**Business Plan (4 hours)** 3.1 Creation of Business Plan Assignment Submission : Presentation of Lean Canvas	4	8
4	**Intellectual Property Rights** 4.1 Trademark 4.2 Copyright	5	8

	4.3 Design 4.4 Patent Assignment Submission : Patent Draft and registration form for Trademark, Copyright, Design and Patent		
5	**Company Formation** 5.1 Promoters, Capital, Shareholders 5.2 Directors, DIN 5.3 Company Name, Registrations 5.4 Branding Assignment Submission : Virtual Company registration	6	8
	Five Assignments Marks		40

References :

[1] "Elements of Entrepreneurial Expertise (New Horizons in Entrepreneurship Series)" by SarasSarasvathym, Publisher : Edward Elgar Publishing.

[2] "Business Model Generation **:**A Handbook for Visionaries, Game Changers, and Challengers" by Alexander Osterwalder

[3] "Value Proposition Design: How to create Products and Services Customers Want" by Alex Osterwalder, Yves Pigneur, Greg Bernarda, Alan Smith, Trish Papadakos

[4] "Writing Winning Business Plans" by Garrett Sutton. Publisher: RDA Press

[5] "Patent Law" by P. Narayanan. Publisher :Eastern Law House, 1975.

[6] "Company Law Procedures" by M.C. Bhandari, LexiNexis, 2018

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ABL 5: Financial Planning, Taxation Policies and Investment

Financial Planning: It is possible to manage income more effectively through financial planning. Managing income helps to understand how much money is required for tax payments, other expenditures and savings. It increases cash flows by carefully monitoring the spending patterns and expenses. Knowledge of comprehensive financial planning will help students to make right financial decisions in their life. It gives guidance in helping choose the right types of investments to fit needs, personality, and goals of their life. In this activity students need to prepare the financial plan for their life.

Taxation Policies: Taxes are levied in almost every country of the world, primarily to raise revenue for government expenditures, although they serve other purposes as well. The simple fact in economics is that there are certain common public goods and public needs that require some form of government and regulation to provide or promote. Taxation is the way to pay for these common goods. In this activity student will learn various types of taxes like Income tax, Corporate tax, Capital gains, Property tax, Inheritance and Sales tax.

Investments: Investments are important because in today's world, just earning money is not enough. But that may not be adequate to lead a comfortable lifestyle or fulfil our dreams and goals. Money lying idle in the bank account is an opportunity lost. Therefore students should have a knowledge to invest money smartly to get good returns out of it. This activity will give insight to the students about investment in the form of Stocks, Mutual Funds, Fixed Deposits, Recurring Deposit, Public Provident Fund, **Employee Provident Fund and National Saving Schemes.**

Methodology: Guest lectures by professionals shall be arranged on Financial Planning, Taxation Policies and Investments. At least one session on each topic shall be taken. Assessment shall be based on performance in following activities:

1. Prepare financial plan
2. Filling of 'Income Tax Return' (Perquisite: Pan Card (if not available, student should apply for pan card)
3. Prepare investment plan

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELP81	Category I :Major Project I	--	--	10	--	--	5	5
		Examination Scheme						
		ISE		MSE	ESE		Total	
		Phase-I:40 Phase-II:40		--	20		100	

The main intention of Major Project is to enable students to apply the knowledge and skills learned in various courses to solve/implement predefined practical problem mainly addressing the issues of society, an industry or a research. These students have already undergone project assignment in their pre-final year in Action Research Plan I & Action Research Plan II courses. Therefore Major Project work may be based on the knowledge gained in the courses OR may be beyond the scope of curriculum of courses taken OR may be extension of the work done in Action Research Plan I and Action Research Plan II courses in pre-final year. The project area may be selected in which the student intend to do further education and/or may be either intending to have employment or self-employment. However thrust should be

- Learning additional skills, computational techniques etc.
- Development of ability to define, design, analyze and implement solution to the problem.
- Deliverable in the form of working prototype of hardware/software OR research publication in a reputed Conference/Journal OR patent
- Learn the behavioral science by working in a group.

Students of final year are categorized as Category I (Internship) and Category II (Non-Internship) students. In final year these students groups will have to execute Major Projects. Execution and evaluation of Major Project will be done as Major Project I and Major Project IIin respective semesters of Category I &Category II students. If a Guide and a group of students of a particular Major Project wish then they can continue the work done as Major Project I and Major Project IIin respective semesters as a part of Major Project. Execution and evaluation of Major Project will be done as per the Project Process developed at Institute level**.** The details of this process are available in Project Log Book.

At the end of Sem VI; students are required to finalize whether they wish to opt Category I (Internship) OR Category II (Non-Internship). Since these are separate group of students; students are required to form a Project Group within the category they have opted for. In order for the smooth execution and evaluation of Major Project; formation of a Project Group from students belonging to different categories will not be allowed at any circumstances. However in order to promote execution of interdisciplinary project; students from different departments but from the same category may execute the Major Project after the approval/agreement from respective Guides.

Evaluation of these Project Groups will however be done on the basis of the work assigned to them OR their project objectives. Project group of maximum three students will be allowed. Each project

group will be completing a comprehensive project work based on the knowledge acquired from the courses studied. Each group will be assigned one faculty as a Guide as per Department policies.

The project work will be internally evaluated in Phases (Phase I and Phase II) by the Expert Groups in the Department consisting of Guide and two OR more than two domain expert faculties based on Scheme of examination for ISE Marks and on the basis of rubrics defined for each Phase of evaluation as per following but not limited to:

- Scope and objectives of the project work.
- Extensive Literature survey.
- Ethics and Societal Aspects
- Planning and Progress of the work (Continuous assessment).
- Design, implementation, and analysis of the project work
- Results, conclusions and future scope
- Report in prescribed format

In order to keep proper evaluation record of the progress of project in the department; each Project Group should submit soft copy of report (approved by respective Guide) in the prescribed format of the Department before each phase of evaluation for ISE marks and one hard copy of the Report duly signed by respective Guide in prescribed format for ESE marks to Project co-ordinator.

For ESE Marks; an approved external examiner and internal examiner appointed by the head of the department together will assess the Major Project during oral examination. The oral examination is a presentation by the group members on the project along with demonstration of the work done. Each individual student should be assessed for his/her contribution, understanding and knowledge gained, the rubrics defined by department and Report in prescribed format for the awards of ISE and ESE marks.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELP71	Category I : Major Project II	--	--	10	--	--	5	5
		Examination Scheme						
		ISE		MSE	ESE		Total	
		Phase-III:40 Phase-IV:40		--	20		100	

The final year students have already under gone first stage of Major Project I and if project guide approves the continuation of same project then students can do so. Otherwise this project is considered as a separate project and students need to do literature survey, define problem, title of the project and objectives of project.

The project work will be internally evaluated in Phases (Phase III and Phase IV) by the Expert Groups in the Department consisting of Guide and two OR more than two domain expert faculties based on Scheme of examination for ISE Marks. There will be Technical Paper Presentation (TPP) event conducted by R&D Cell and Project Exhibition (PE) event conducted by respective Departments as per the academic time table. Participation in these activities is mandatory. After evaluation Winners will be declared from TPP and PE events separately as per the rubrics, rules and regulations framed by R&D Cell and Department respectively.
In order to keep proper evaluation record of the progress of project in the department; each Project Group should submit soft copy of report (approved by respective Guide) in the prescribed format of the Department before each phase of evaluation for ISE marks and one hard copy of the Report duly signed by respective Guide in prescribed format for ESE marks to Project co-ordinator.

The department should keep proper evaluation record of the progress of project and at the end of the semester it should be assessed for awarding ISE marks. The ISE Marks should be examined by approved internal faculty appointed by the head of Department on the basis of rubrics defined for each Phase of evaluation as per following but not limited to:

- Scope and objectives of the project work.*
- Extensive Literature survey.*
- Ethics and Societal Aspects
- Planning and Progress of the work (Continuous assessment)
- Design, implementation, and analysis of the project work.
- Results, conclusions and future scope.
- Report in prescribed format.

(*NOT required if Major Project II is not in continuation of Major Project I)

For ESE Marks; an approved external examiner and internal examiner appointed by the head of the department together will assess the Major Project during oral examination. The oral examination is a presentation by the group members on the project along with demonstration of the work done.

Each individual student should be assessed for his/her contribution, understanding and knowledge gained and the rubrics defined by department for awarding ISE and ESE marks.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELP71	Category II : Major Project I	--	--	10	--	--	5	5
		Examination Scheme						
		ISE		MSE	ESE		Total	
		Phase-I:40 Phase-II:40		--	20		100	

The main intention of Major Project is to enable students to apply the knowledge and skills learned in various courses to solve/implement predefined practical problem mainly addressing the issues of society, an industry or a research. These students have already undergone project assignment in their pre-final year in Action Research Plan I & Action Research Plan II courses. Therefore Major Project work may be based on the knowledge gained in the courses OR may be beyond the scope of curriculum of courses taken OR may be extension of the work done in Action Research Plan I and Action Research Plan II courses in pre-final year. The project area may be selected in which the student intend to do further education and/or may be either intending to have employment or self-employment. However thrust should be

- Learning additional skills, computational techniques etc.
- Development of ability to define, design, analyze and implement solution to the problem.
- Deliverable in the form of working prototype of hardware/software OR research publication in a reputed Conference/Journal OR patent
- Learn the behavioral science by working in a group.

Students of final year are categorized as Category I (Internship) and Category II (Non-Internship) students. In final year these students groups will have to execute Major Projects. Execution and evaluation of Major Project will be done as Major Project I and Major Project IIin respective semesters of Category I &Category II students. If a Guide and a group of students of a particular Major Project wish then they can continue the work done as Major Project I and Major Project IIin respective semesters as a part of Major Project. Execution and evaluation of Major Project will be done as per the Project Process developed at Institute level**.** The details of this process are available in Project Log Book.

At the end of Sem VI; students are required to finalize whether they wish to opt Category I (Internship) OR Category II (Non-Internship). Since these are separate group of students; students are required to form a Project Group within the category they have opted for. In order for the smooth execution and evaluation of Major Project; formation of a Project Group from students belonging to different categories will not be allowed at any circumstances. However in order to promote execution of interdisciplinary project; students from different departments but from the same category may execute the Major Project after the approval/agreement from respective Guides.

Evaluation of these Project Groups will however be done on the basis of the work assigned to them OR their project objectives. Project group of maximum three students will be allowed. Each project group will be completing a comprehensive project work based on the knowledge acquired from the courses studied. Each group will be assigned one faculty as a Guide as per Department policies.

The project work will be internally evaluated in Phases (Phase I and Phase II) by the Expert Groups in the Department consisting of Guide and two OR more than two domain expert faculties based on Scheme of examination for ISE Marks and on the basis of rubrics defined for each Phase of evaluation as per following but not limited to:

- Scope and objectives of the project work.
- Extensive Literature survey.
- Ethics and Societal Aspects
- Planning and Progress of the work (Continuous assessment).
- Design, implementation, and analysis of the project work
- Results, conclusions and future scope
- Report in prescribed format

In order to keep proper evaluation record of the progress of project in the department; each Project Group should submit soft copy of report (approved by respective Guide) in the prescribed format of the Department before each phase of evaluation for ISE marks and one hard copy of the Report duly signed by respective Guide in prescribed format for ESE marks to Project co-ordinator.

For ESE Marks; an approved external examiner and internal examiner appointed by the head of the department together will assess the Major Project during oral examination. The oral examination is a presentation by the group members on the project along with demonstration of the work done. Each individual student should be assessed for his/her contribution, understanding and knowledge gained, the rubrics defined by department and Report in prescribed format for the awards of ISE and ESE marks.

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Course Code	Course Name	Teaching Scheme (Hrs/week)			Credits Assigned			
		L	T	P	L	T	P	Total
ELP81	Category II: Major Project II	--	--	10	--	--	5	5
		Examination Scheme						
		ISE		MSE	ESE		Total	
		Phase-III:40 Phase-IV:40		--	20		100	

The final year students have already under gone first stage of Major Project I OR Major Project II work in their respective semesters and in this semester students are expected to continue the project work of stage I then they need to separately carry literature survey, define problem, title of the project and objectives of project.

The project work will be internally evaluated in Phases (Phase III and Phase IV) by the Expert Groups in the Department consisting of Guide and two OR more than two domain expert faculties based on Scheme of examination for ISE Marks. There will be Technical Paper Presentation (TPP) event conducted by R&D Cell and Project Exhibition (PE) event conducted by respective Departments as per the academic time table. Participation in these activities is mandatory. After evaluation Winners will be declared from TPP and PE events separately as per the rubrics, rules and regulations framed by R&D Cell and Department respectively however ISE marks are not allotted for these activities. In order to keep proper evaluation record of the progress of project in the department; each BE Project Group should submit soft copy of report (approved by respective Guide) in the prescribed format of the Department before each phase of evaluation for ISE marks and one hard copy of the Report duly signed by respective Guide in prescribed format for ESE marks to Project co-ordinator.

The department should keep proper evaluation record of the progress of project and at the end of the semester it should be assessed for awarding ISE marks. The ISE Marks should be examined by approved internal faculty appointed by the head of Department on the basis of rubrics defined for each Phase of evaluation as per following but not limited to:

- Scope and objectives of the project work.*
- Extensive Literature survey.*
- Ethics and Societal Aspects
- Planning and Progress of the work (Continuous assessment)
- Design, implementation, and analysis of the project work.
- Results, conclusions and future scope.
- Report in prescribed format.

(*NOT required if Major Project II is not in continuation of Major Project I)

For ESE Marks; an approved external examiner and internal examiner appointed by the head of the institute together will assess the Major Project during oral examination. The oral examination is a presentation by the group members on the project along with demonstration of the work done.
Each individual student should be assessed for his/her contribution, understanding and knowledge gained and the rubrics defined by department for awarding ISE and ESE marks.