(2) From remaining **six** questions solve any **four** questions.
(3) Assume **suitable** additional data if **required**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Design a circuit to implement the following function using a Type–1 MUX design :—   8
        $F(A, B, C, D, E) = \sum m(0, 5, 7, 11, 15, 16, 18, 25, 29)$.

    (b) For the logic diagram shown in the **figure** below carry out the detailed analysis (including   12
        state diagram). X is the input signal and Z is output signal.
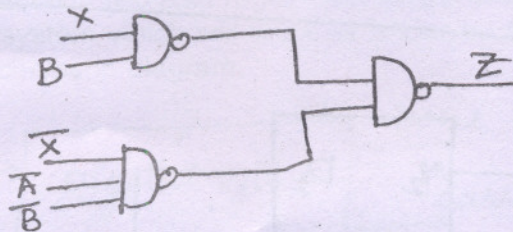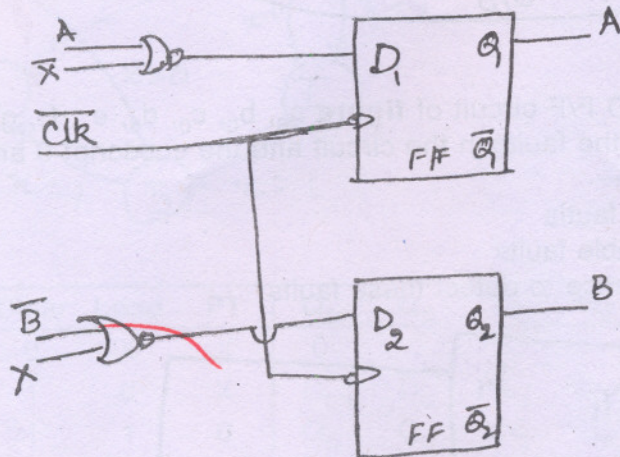

2. (a) Explain the path sensitization method of fault detection and location. What are the advantages   10
        and disadvantages of the path sensitization method ? Use this method for the following
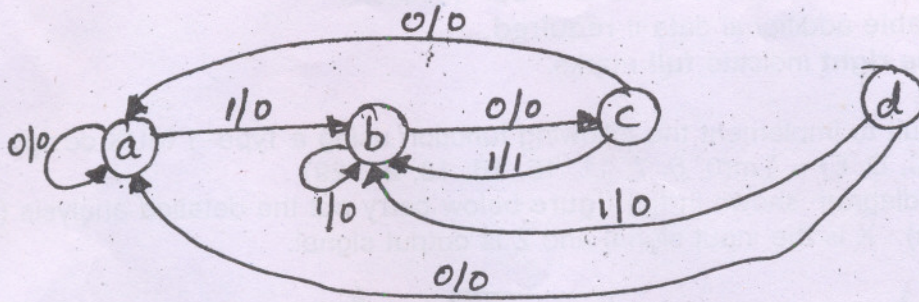   circuit :—
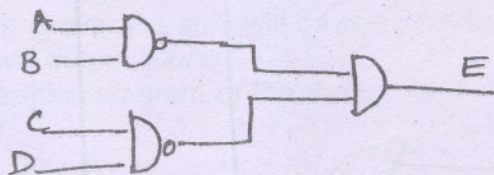
    (b) Implement the following sets of functions using a decoder and some gates. Design the   10
        logic for minimum chip count.
        $F_1(A, B, C) = \sum m (0, 1, 2)$
        $F_2(A, B, C) = \sum m (1, 2, 3, 4, 5, 7)$
        $F_3(A, B, C) = \sum m (2, 3, 5, 7)$.

3. (a) The incoming serial data is to be detected in overlapping mode for the sequence 10110   12
        The output Z is asserted high when the sequence is received. Draw the state diagram and
        realize the logic using D-flip-flops and gates.

    (b) For the circuit given below determine the number of logic hazards. What product terms are   8
        necessary to eliminate these logic hazards ? Write the logic hazard free function for the
   circuit.
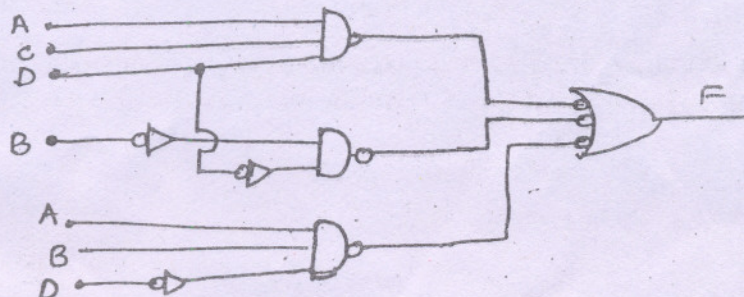
[**TURN OVER**

4. (a) Design a circuit to implement a BCD to 2421 code converter using PAL. The signal list is   **8**
        $F_3, F_2, F_1, F_0, I_3, I_2, I_1, I_0$.

  (b) Minimize the state diagram in **figure** given below and implement the logic using D-flip-flops   **12**
        and gates.

5. Consider the following faults of the D F/F circuit of **figure** $a_0, b_0, c_0, d_0, e_1, f_1, g_1, h_1$ where   **20**
a, b ...., h denote the location of the faults in the circuit and the subscript 0 and 1 denote
s–a–0 and s–a–1 faults respectively —

  (a) Determine the undetectable fautls

  (b) Determine the indistinguishable faults

  (c) Find the optimum test sequence to detect these faults
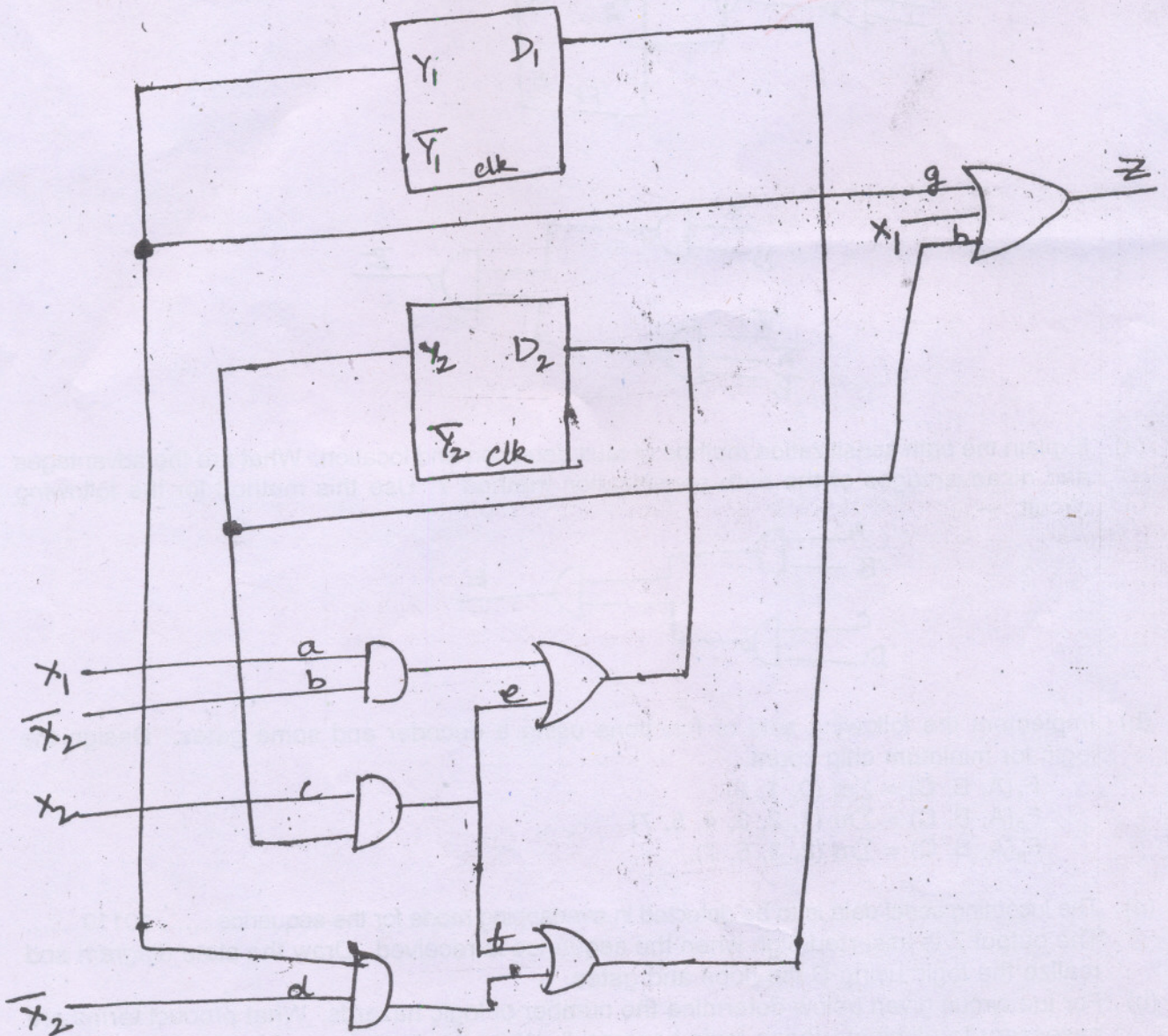
6.   State diagram for a sequential network is shown below. Realise the network using IC 745163   **20**
     and PLA. Use the order Q_D, Q_C, Q_B, Q_A for the state variables. Operation of 745163 is also
     shown :—
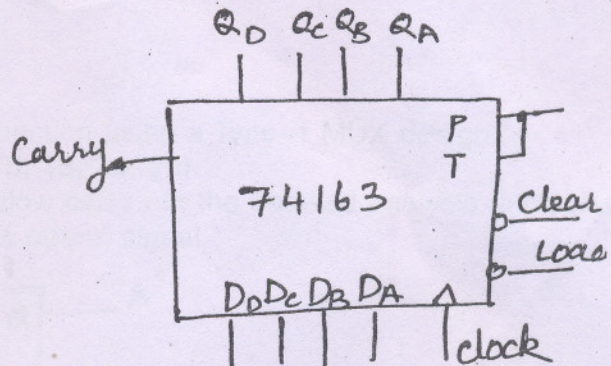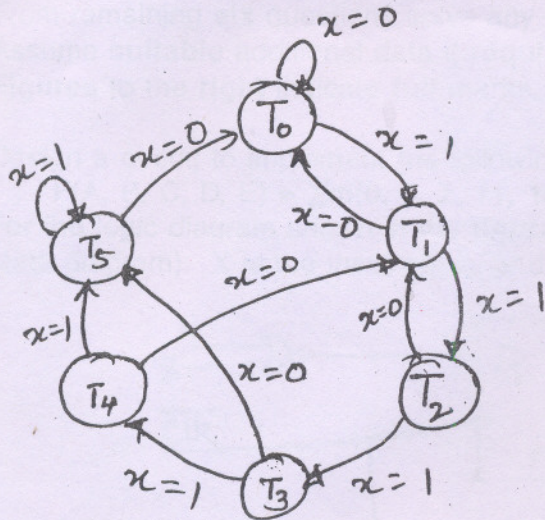
Clear	Load	PT	Q_D	Q_C	Q_B	Q_A	
0	X	X	0	0	0	0	(Clear)
1	0	X	D_D	D_C	D_B	D_A	(Load)
1	1	0	Q_D	Q_C	Q_B	Q_A	(No change)
1	1	1	Present State +1				(Increment count)

7.   Two four bit numbers are loaded in two shift registers X and Y which are part of a digital system.   **20**
     It is desired to design this system which will work as a four bit serial adder. The input-output
     signals are shown in the Schematic diagram.
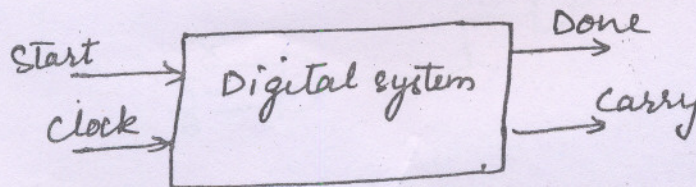
On receiving 'start' it will begin the serial operation of adding the numbers in the registers X and
Y. After the operation is over the sum will be stored in the register X, the carry will be available
as an output and it will output 'Done'.

Make a functional partition diagram of the system and MDS diagram of its controller.
Design the controller.