

M.E. (ETRX) Sem I (R)  
Digital System Design

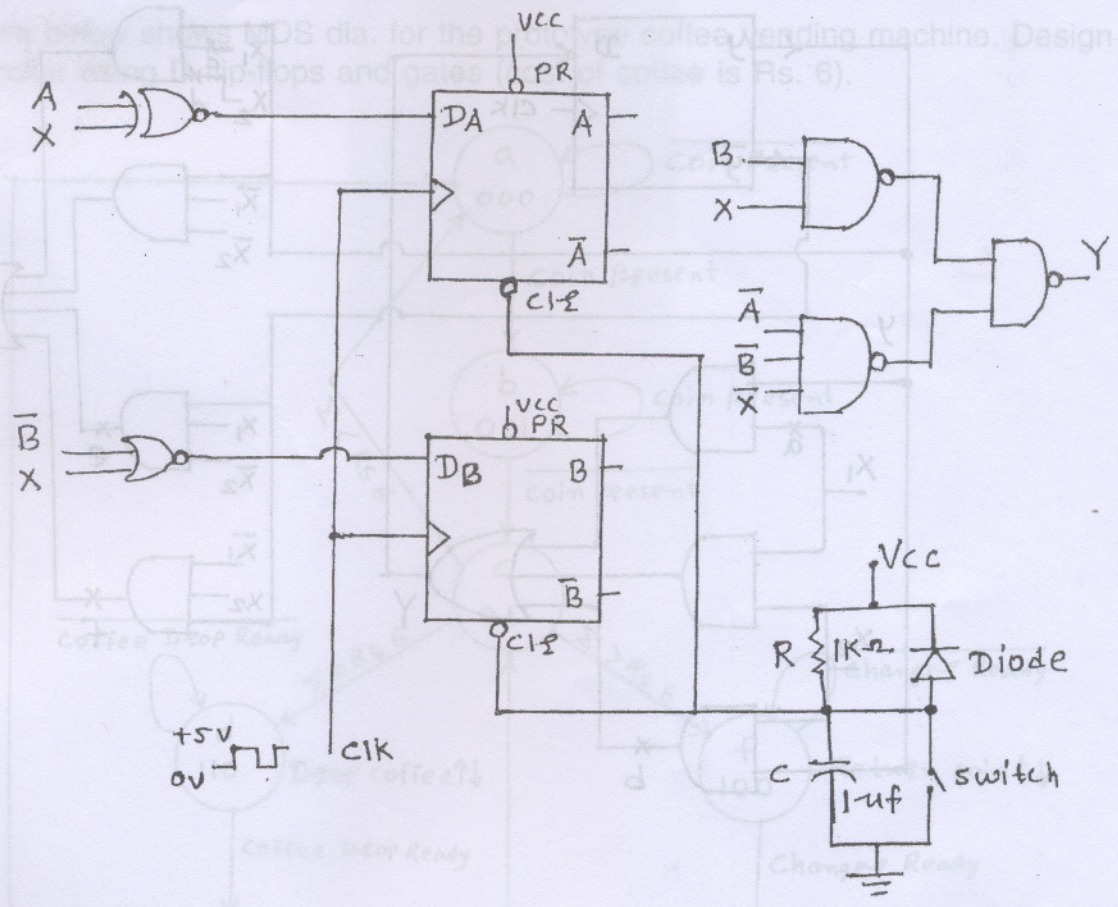
21/12/09  
BB-6116

Con. 5276-09.

(4 Hours) [Total Marks : 100]

- N.B. : (1) Question No. 1 is **compulsory**.  
(2) Attempt any **four** out of remaining **six** questions.  
(3) Assume **suitable** additional data if **required**.  
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Develop a ROM for BCD to Excess 3 code converter. 8  
(b) Use demux with active low O/Ps and gates with Fan in 2 to realize the function— 6  
 $Y = F(A, B, C) = \sum m(0, 3, 4, 6)$   
(c) Realize the following function with type 2 mux design method and only one inverter :- 6  
 $Y = F(A, B, C, D) = \sum m(0, 1, 2, 3, 9, 11, 12, 13)$
2. Design a logic ckt that will give O/P high when invalid BCD code arrives in the form of serial data. 20
3. (a) For the logic diagram shown in following **figure**, carry out the detailed analysis 10  
(Including state dia and power on reset ckt). X is i/p and Y is o/p signal.



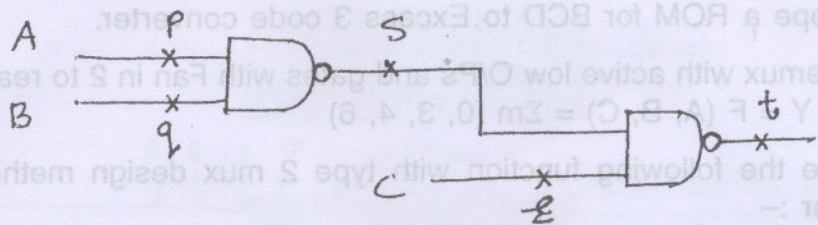
- (b) Design BCD to seven segment code converter using PAL. Give specifications of the PAL. 10



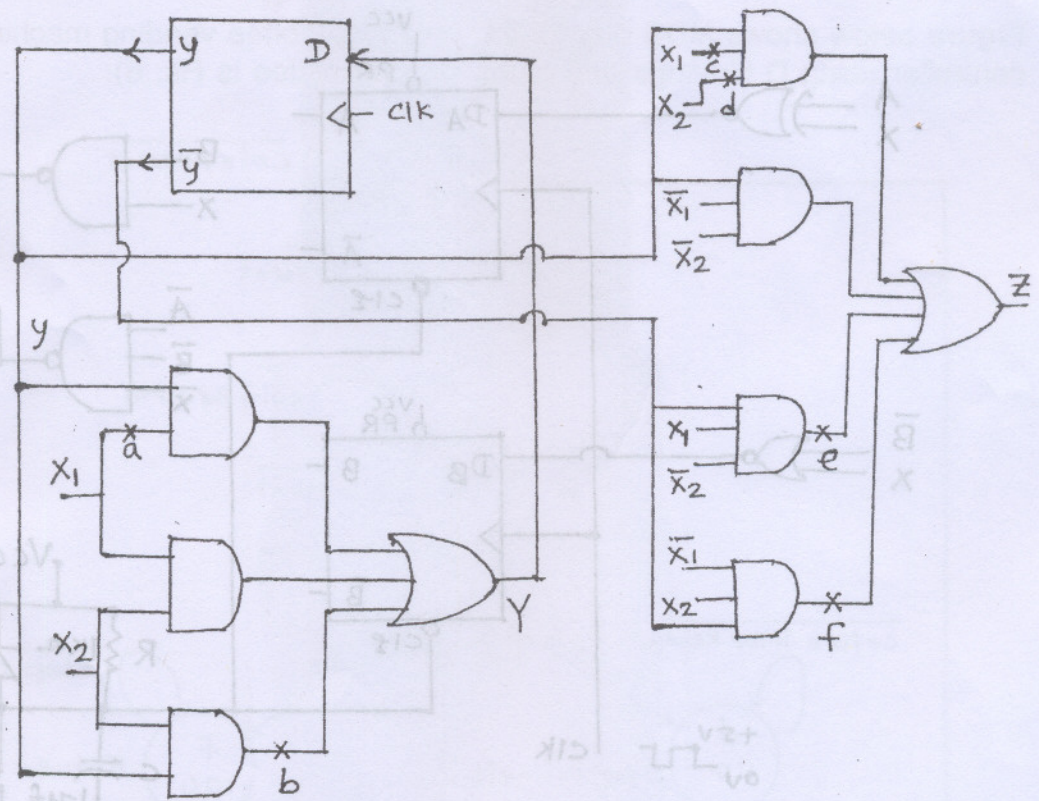
4. (a) For logic circuit whose Boolean equation is given below, find all logic hazards. 10  
How will you eliminate these logic hazards ?

$$F = ABC\bar{C} + (A + B) (\bar{A} + \bar{D})$$

- (b) For following combinational n/w, obtain a test set covering all the possible faults- 10

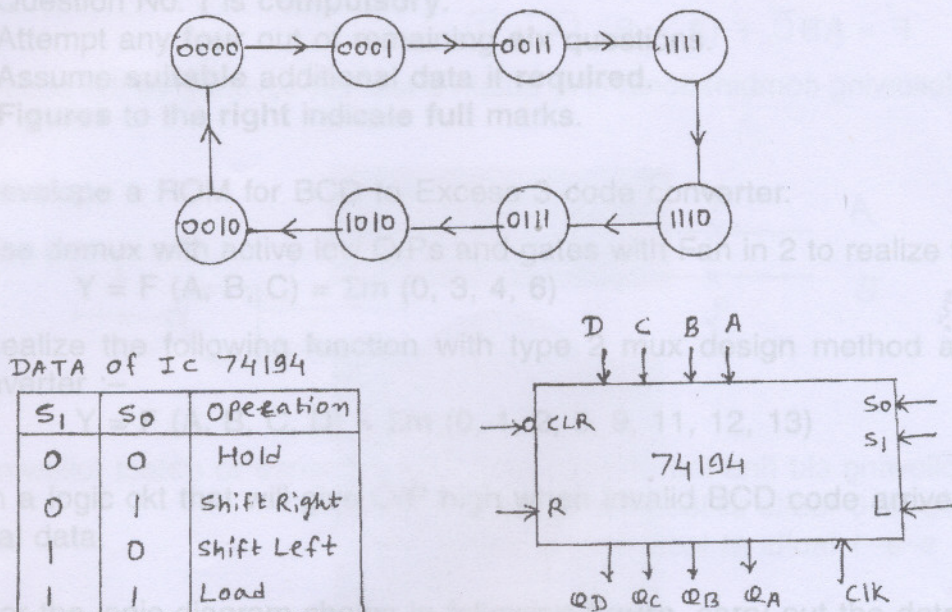


5. For the following ckt find the shortest possible sequence to detect following faults :- 20  
(a) s-a-0 faults at locations a, c, d  
(b) s-a-1 faults at locations b, e, f





6. A synchronous sequential ckt having 4 bits o/p, follow through following sequence. 20  
Design the ckt using shift register IC 74194 and PLA.



7. Figure below shows MDS dia. for the prototype coffee vending machine. Design the controller using D flip-flops and gates (cost of coffee is Rs. 6). 20

