M.E. (ETRX) Sem II (R)
VLSI Design

Con. 5062-09. **BB-6162**

(4 Hours) **[Total Marks : 100**

216

14-12-09

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any **suitable** data wherever **required** but justify the **same**.

1. (a) For obtaining symmetrical characteristics comment on the aspect ratios of load and the driver. If the mobility ratio of electron to holes is 3:1. **20**
   (b) CMOS NAND with CMOS NOR gate based on different parameters.
   (c) Butted and Buried contacts in VLSI
   (d) Skew rate in case of VLSI Design.
   (e) Define super-buffer and state the need of the same.

2. (a) Derive expression for drain current in nMOS device. **10**
   For a nMOS device if —
   $\mu_n = 520\ cm^2 / V\text{-sec}$ $t_{ox} = 12$ nm
   $\varepsilon_{0x} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}\ F / cm$ $W = 1{\cdot}2\mu m$ $L = 0{\cdot}5\ \mu m$
   $V_G = -5$ Volts $V_{THp} = -1{\cdot}5$ Volts
   Find Drain current if $V_{DS} = -2$ Volts.
   State the condition in which the transistor is in and explain why ?
   (b) Find the expression for Threshold voltage of nMOS device also explain the effect of substrate potential (Body Effect) on Threshold. **10**
   Find the threshold shift due to body effect.
   Where $V_{SB} = 3$Volts $N_A = 3 \times 10^{16}\ cm^{-3}$ $t_{ox} = 300°\ A$
   $\varepsilon_0 = 8{\cdot}85 \times 10^{-14}$ $\varepsilon_{0X} = 3{\cdot}9\ \varepsilon_0$ $\varepsilon_{si} = 11{\cdot}7\ \varepsilon_0$
   $n_i = 1{\cdot}5 \times 10^{10}\ cm^{-3}$ $q = 1{\cdot}6 \times 10^{-19}\ C$

3. (a) Compare enhancement and depletion type of loads used in nMOS Inverter circuit. Draw proper diagram. State clearly the different parameters which characterize each type of Inverters. **10**
   (b) Explain in great detail the transfer characteristics of CMOS Inverter. Draw the transfer characteristics and explain all five regions clearly. **10**

4. (a) $F = \overline{a + (b\ .\ c.\ d)}$ **10**
   Consider the logical function as given above
   (i) Design the CMOS logic gate that provides the function.
   (ii) Is it possible to find an Euler graph for the circuit ? If so, construct the graph and also draw stick diagram and layout.
   (b) What is total power dissipation in case of CMOS Inverter ? Discuss how to approximate the estimation of total power dissipation ? Derive expression for short circuit power dissipation for CMOS Inverter. **10**

5. (a) CMOS Inverter device is to be fabricated, describe its fabrication steps giving the mask sequence. Sketch the masking steps in cross-section view. **10**
   (b) What is sheet resistance ? **10**
   Find resistance Rn for nMOS if electron mobility $\mu_n = 560\ cm^2 / V\text{-sec}$,
   $t_{OX} = 10$ nm, $\varepsilon_{0X} = 3{\cdot}9 \times 8{\cdot}85 \times 10^{-14}$ F/cm, and $V_G = 3{\cdot}3$ Volts, $V_{THp} = 0{\cdot}7$ Volts —
   (i) if $W = 10\ \mu m$ $L = 0{\cdot}5\ \mu m$
   (ii) if channel width is increased to a value of $W = 22\ \mu m$ while the Channel length remains same.

6. (a) What is pass transistor ? State advantages of transmission gate. Explain the method to design 8:1 MUX using nMOS. Also draw stick diagram for the same. **10**

   (b) What is significance of scaling ? Its requirement and limitations. Explain various methods of scaling and compare them. **10**

7. Write short notes on any **four** of the following :— **20**

   (a) Design Rules and its Significance
   (b) Testability in case of VLSI
   (c) Hot Electron Effect
   (d) Latch up Problem in CMOS
   (e) Photolithography.
