BE - SEM VII (R-2012) (CBSGS) Dec 2015

ETRX

OFC

QP Code : 6151

(3 Hours) [Total marks : 80

N.B.
1) Question No-1 is Compulsory.
2) Attempt any Three (03) Questions from remaining Five (05) Questions.
3) Assume suitable data where ever necessary.

Q. No.		Marks.
Q.1	**Attempt the following Questions(any4)**	
	a) What are the advantages of optical fiber communication?	5
	b) Compare step Index Fiber and graded index fiber?	5
	c) What do you understand by double heterostructure? State its limitations	5
	d) Explain the different types of losses in optical fiber communication	5
	e) What is Optical Transport network (OTN)	5
	f) Define Bandwidth Distance Product	5
Q.2(a)	Explain any one of the fiber fabrication process with neat diagram ,Compare the different methods of fabrication	8
Q.2(b)	A silica optical fiber with core diameter large enough to be considered by ray theory has a core refractive index of 1.5 and cladding refractive index of 1.47 Determine –(i)The critical angle (ii)The NA (iii)The Acceptance Angle	6
Q.2(c)	Explain a the application of Optical Amplifiers, for th FA give details Architecture with possible configurations and power conversion efficiency and gain	6
Q.3(a)	Explain the different types of losses in optical fiber communication ,Give the various factors responsible for optical signal attenuation &Dispersion	8
Q.3(b)	Compare the electrical and optical bandwidth for an optical fiber communication system and develop relationship between them	6
Q.3(c)	Name five connectors used in optical fiber communication, State the difference between couplers and connectors	6
Q.4(a)	Define the quantum efficiency and responsivity of photo detector, Derive the expression for responsivity of intrinsic photo detector in terms of quantum efficiency of the device and wavelength of the incident radiation, Determine the wavelength at which the quantum efficiency and responsivity are equal.	8
Q.4(b)	Explain with block schematic of optical fiber soliton transmission system with optical soliton pulses (i)collision of two solitons (ii)Four stable solitons at safe separation distance.	6
Q.4(c)	Difference between following term in context with optical communication(i)Optical Source &Optical Detector (ii)Coherent and Non coherent optical transmission	6
Q.5(a)	Describe the structure and operation of OTDR with illustration of possible back scatter plot from a fiber under test.	8
Q.5(b)	Explain the term protocol and Internet protocol(IP),using OSI reference model discuss implementation aspect of the (i)SONET(ii)DWDM	6
Q.5(c)	Explain with components a typical WDM link and some performance measurement parameter of user interest	6
Q.6	Write short note on(any4): (a) Optical Coupler and Application (b)Nearest Neighbor & Long Distance Link power Budget (c)Optical safety &Service Interface (d)Optical Switches (e)Structures for InGaAS APDs	20

B-E Sem III K-2007 Electronics
Comm. Networks

QP Code : **2493**

(3 Hours) [Total Marks :100

N.B. : (1) Question no. 1 is **compulsory.**
(2) Answer any **four** out of the remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. Answer any four:-
   (a) Explain functions of data link layer 5
   (b) What are the advantages of fiber optic as communication medium 5
   (c) Explain general principles of congestion control in communication network 5
   (d) Explain various LAN topologies 5
   (e) Explain TSI switch. 5

2. (a) Explain ADSL technology in detail 10
   (b) Differentiate circuit switching, packet switching and message switching. Draw suitable diagrams. 10

3. (a) Explain OSI reference model and functions of each layer. 10
   (b) With the reference to HDLC, explain the data transfer modes, frame structure and different types of frames 10

4. (a) Explain different types of ARQ and compare their merits and demerits. 10
   (b) Explain IEEE 802.3 and LAN architecture and MAC layer frame format. 10

5. (a) What is meant by Flow control? Explain sliding window protocol. 10
   (b) What are transmission impairements? Explain and compare co-axial cable, twisted pair cable and fiber optic cable. 10

6. (a) Explain various error detection techniques. 10
   (b) What are different types of routing algoritahms? Explain any one in detail. 10

7. (a) Explain the following network connecting devices 10
   (i) Switch (ii) Router (iii) Gateway
   (iv) Hub (v) Bridge
   (b) Write a short notes on (any two):-
   (i) Berkeley API 5
   (ii) Space division switching 5
   (ii) ISDN 5

BE - SEM VII (R-2007) - ETRX
& OTR
VLSI Design

Dec 2015

QP Code : 2373

(3 Hours) [Total Marks: 100]

N.B.: (1) Question No. 1 is compulsory.
(2) Attempt any four questions out of remaining six questions.
(3) Assume suitable data wherever required.

Q.1 Attempt any Four questions.

(a) Explain the effect of channel length modulation on the Current- Voltage characteristics of an nMOS transistor. (20)

(b) Differentiate between the process of diffusion and ion implantation.

(c) State and plot the design rule for implant mask in NMOS technology and the problems faced in case of violation of the rule.

(d) Design a 2:1 MUX using CMOS transmission gate logic and write Verilog module for the circuit designed.

(e) Explain the importance of noise margins in an inverter circuit.

Q.2 (a) For an n-channel MOS transistor draw the charge distribution diagram, energy band diagram and the Fermi level under the following conditions: at thermal equilibrium, under accumulation and under strong inversion. (10)

(b) Explain the different regions of operation in the voltage transfer characteristics of a CMOS inverter. (10)

Q.3 (a) Describe the fabrication steps giving the mask sequence for the fabrication of an NMOS transistor with the help of cross sectional view of all the masking steps. (10)

(b) Draw the schematic and stick diagram for the following Boolean function in CMOS logic: $Y = AB + C.(D+E)$ (10)

Q.4 (a) Draw the stick diagram and mask layout of a depletion load NMOS inverter using lambda based design rules. (10)

(b) Derive the expressions for the critical voltages V_{OL}, V_{OH}, V_{IL} and V_{IH} of a resistive load NMOS inverter. (10)

Q.5 (a) Compare the full scaling and constant voltage scaling models of MOSFETs. Demonstrate the effects of scaling on the area, delay, power consumption and current density of the device. (10)

(b) Consider an Al-SiO_2-n-type Si MOS structure with the following parameters: (10)
$N_D = 2.5 \times 10^{14}$ /cm^3, $Q_{OX} = 10^{10}$q /cm^2, $t_{OX} = 650$ A°, $\phi_{ms} = -0.35$ V
Find the zero bias threshold voltage, V_{T0}. Calculate the Ion implant dose necessary to change the threshold voltage from V_{T0} to +1V.

Q.6 (a) Design a half adder, a full adder using half adders and primitive gates and a 4-bit ripple carry adder using full adders. Write Verilog modules for the circuits designed. (10)

(b) Explain CMOS latch up and the strategies used for its prevention. (10)

Q.7 Write short notes on any Two (20)

(a) MOS C-V Characteristics

(b) Short channel effects

(a) Power dissipation in CMOS circuits

BE- SEM VII (R-2012) (CBSGS)
ETRX
Dec 2015

A. I.

Q.P. Code : **6145**

(3 Hours)

[Total Marks : 80

N.B. : (1) Question **No.1** is **compulsory**.
(2) **Attempt** any **three** questions from remaining questions.
(3) **Assume** suitable **data** whevevre **necessary**.

1. Attempt any four questions : 20
   (a) Compare and contrast the biological neuron and artificial neurons.
   (b) Define fuzzy logic and crisp logic. With suitable examples, explain the operations and properties of fuzzy sets, crisp sets, fuzzy relations and crisp relations.
   (c) What are the various activation functions and learning rules used in neural networks?
   (d) Explain any two types of De-fuzzification methods.
   (e) Draw a McCulloch-Pitts neuron and explain its working.

2. (a) Differentiate between supervised and unsupervised learning methods. 10
   (b) Design a Hopfield network for 4-bit bipolar patterns. The training patterns are : 10

$S_1 = [1,-1,-1,-1]$
$S_2 = [-1,1,1,-1]$
$S_3 = [-1,-1,-1,1]$

   Find weight matrix and energies for three input samples. Determine the pattern to which the sample S = [-1, 1,-1,-1] associates.

3. (a) What are the two types of BAM? Explain. How are the weights determined in a discrete BAM. 10
   (b) Find the weights required to perform the following classification using Perceptron network. The vectors (1,1,1,1) and (-1,1,-1,-1) are belonging to the class and have target value 1 and vectors (1,1,1-1) and (1 ,-1 ,-1, 1) are not belonging to the class and have a target value -1. Assume learning rate as 1 and initial weights as 0. 10

4. (a) With a neat architecture, explain the training algorithm of Kohonen self-organizing maps. 10
   (b) State the importance of back propagation algorithm and draw its architecture. 10

TURN OVER

5. (a) For the fuzzy sets A, B and C are define on discrete universe X, Y and Z repectively. 10

$$A = \left\{\frac{0.1}{x_1} + \frac{0.5}{x_2} + \frac{1.0}{x_3}\right\}, B = \left\{\frac{0.3}{y_1} + \frac{0.8}{y_2}\right\}, A = \left\{\frac{0.4}{z_1} + \frac{0.7}{z_2} + \frac{1.0}{z_3}\right\}$$

Find:

(i) Fuzzy Cartesian product P = A X B;

(ii) Fuzzy Cartesian product S = B X C;

(iii) T=P O S using min-max and max-product method.

(b) With a neat architecture, explain the training algorithm and testing algorithm of Adaline network. 10

6. Write short notes on any four : 20

(a) Simulated annealing,

(b) LVQ,

(c) Fuzzy Logic Controller,

(d) Boltzmann Machine,

(e) Adaptive Resonance Theory.

BE-SEM VII (R-2012) (CBSGS) Dec 2015
EXTC
ASIC Verification

Q.P.Code No: **6148**

(3 Hours) **[Total marks : 80**

N.B.: 1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve the following (Any Four) **20 Marks**

A. Highlight the important features of Virtex-7 FPGA.

B. Explain what we randomize in SystemVerilog and how to check whether randomization is successful or not?

C. What is assertion in systemverilog and what are its advantages?

D. What is DPI-C?

E. Explain Event regions in SV.

Q2. A. Discuss Silicon technology challenges considering Timing closure, Capacity, Physical properties, Design Productivity Gap and Time-to-Market Trends. **05 Marks**

B. Given the following code sample: **05 Marks**

```
bit [7:0] my_mem [3] = '{default:8'hA5};
logic [3:0] my_logicmem [4] = '{0,1,2,3};
logic [3:0] my_logic = 4'hF;
```

Evaluate the following statements in the given order, and give the result for each assignment:

I. my_mem[2] = my_logicmem[4];
II. my_logic = my_logicmem[4];
III. my_logicmem[3] = my_mem[3];
IV. my_mem[3] = my_logic;
V. my_logic = my_logicmem[];
VI. my_logic = my_mem[1];
VII. my_logic = my_logicmem[my_logicmem[4]];

C. For the following class, create: **05 Marks**

1. A constraint that limits read transaction addresses to the range 0 to 7, inclusive
2. Write behavioral code to turn off the above constraint. Construct and randomize a *MemTrans* object with an in-line constraint that limits read transaction addresses to the range 0 to 8, inclusive. Test that the in-line constraint is working.

```
class MemTrans;
  rand bit rw; // read if rw = 0, write if rw = 1
  rand bit [7:0] data_in;
  rand bit [3:0] address;
endclass
```

Q. Explain various data types in Verilog. Write a verilog code to swap contents of two registers with and without a temporary register? **05 Marks**

TURN OVER

Q3. A. Explain the necessity and advantages of using interface. 05 Marks

B. Give comparison between fixed array, associative array, dynamic array and queues. 05 Marks

C. What is "scope resolution operator"? Give suitable example. 05 Marks

D. Explain SystemVerilog Constraint Random Stimulus Generation with suitable example. 05 Marks

Q4. A. With suitable example explain how communication between threads is achieved with fork...join, fork ...join_none and fork...join_any. 05 Marks

B. With respect to SystemVerilog explain the following with suitable example 05 Marks

I. Inheritance

II. Polymorphism

C.

1. Create a task called wait10 that for 10 tries will wait for 10ns and then check for 1 semaphore key to be available. When the key is available quit the loop and print out the time.
2. What is the output with the following code? 05 Marks

```
initial begin
  fork
    begin
        sem = new(1);
        sem.get(1);
        #45ns;
        sem.put(2);
    end
   wait10();
  join
end
```

D. For the following interface, add the following code: 05 Marks

1. A clocking block that is sensitive to the negative edge of the clock, and all I/O that are synchronous to the clock
2. A modport for the testbench called *master* and a modport for the DUT called *slave*
3. Use the clocking block in the I/O list for the *master* modport

Q5. A. Given the following class: 05 Marks

1) Create a method in an extended class ExtBinary that multiplies val1 and val2 and returns an integer.
2) Use the ExtBinary class to initialize val1=15, val2=8, and print out the multiplied value.

```
class Binary;
  bit [3:0] val1, val2;
  function new(input bit [3:0] val1, val2);
    this.val1 = val1;
    this.val2 = val2;
  endfunction
  virtual function void print_int(input int val);
    $display("val=0d%0d", val);
  endfunction
endclass
```

B. Explain with neat diagram the typical formal verification design process with SystemVerilog assertions. 05 Marks

C. With suitable example explain how Inline constraints allows to add extra constraints to already existing constraints which are declared inside class. 05 Marks

D. Write a verification plan for an ALU with: 05 Marks

1. Asynchronous active high input reset
2. Input clock
3. 4-bit signed inputs, A and B
4. 5-bit registered signed output C
5. 4 opcodes
   - i. Add
   - ii. Sub
   - iii. bitwise invert input A
   - iv. reduction OR input B

Q6. A. If Functional coverage is 100% and code coverage is not, then what does it mean? Also explain the concept of cross coverage. 05 Marks

B. Explain the following with suitable example

a. Statement coverage
b. Block coverage 05 Marks

C. With suitable example for each, explain the following with respect to Sequences in assertions:

a. Zero Delay
b. Consecutive Repetition
c. Sequence And
d. Sequence Intersect
e. Sequence Throughout 05 Marks

D. Explain with suitable example interfacing between 'C' and SystemVerilog 05 Marks

BE Sem VII (R-2007)

ETRX Dec 2015

PED

QP Code : **2300**

(3 Hours) [Total Marks :100

N.B. : (1) Question no. 1 is compulsory.
(2) Solve any four questions out of remaining six questions.
(3) Figures to the right indicate full marks.

1. (a) Explain slip S of an induction motor. 5
(b) Differentiate between online ups and off-line ups 5
(c) Explain regenerative braking in DC motor. 5
(d) Differentiate between voltage commutation and current commutation in chopper. 5

2. (a) Explain Basic series inverter with circuit diagram and waveforms. 10
(b) Explain the working of current cumulated chopper with the help of circuit diagram and waveforms. 10

3. (a) Explain the working of forward converter used in SMPS with circuit diagram and waveforms. 10
(b) Explain semiconverter drive to control the speed of DC motor in contineous current mode. Draw torque speed characteristics. 10

4. (a) Explain $\frac{V}{f}$ control scheme to control the speed of AC motor with the help of curves and implementation circuit. 10
(b) What is the effect of harmonics present in inverter output. Discuss the various methods to reduce the harmonics present in inverter output. 10

5. (a) A 210, 1200 rpm, 10 A separately excited motor is controlled by 1 ϕ fully controlled converter with an a.c. source voltage of 230V, 50HZ. Assume that sufficient inductance is present in the armature circuit to make the motor current continuous and ripple free for any torque greater than 25% of rated voltage. $R_a = 1.5\ \Omega$ 10
(i) What should be the firing angle to get the rated torque at 800 rpm
(ii) Compute the firing angle for the rated braking torque-at-1200 rpm
(b) Explain the working of Kramer's drive to control the speed of AC motor for subsynchronous speed. 10

6. (a) Explain class E chopper circuit with the help of waveforms and quadrants of operation 10
(b) What do you understand dual converter. Draw diagram and waveforms. Derive the relation for $\alpha_1 + \alpha_2 = 180^0$ 10

7. Write short notes on (any two):-
(a) Effect of source inductance in fully controlled bridge rectifier 10
(b) Rotor resistance control of induction motor 10
(c) Parallel Inverter. 10

B.E (ETRX) sem VII OLD 14/12/2015

Wireless Communication.

QP Code : 2230

(3 Hours)

Total Marks : 100

N. B.1 Question No-1 is compulsory
2 Figures to the right indicate full marks
3 Solve any four questions out of remaining six questions

Q.1 a) Explain the concept of umbrella cell approach. 5
b) Differentiate between Erlang-B and Erlang-C system. 5
c) Explain spectral efficiency and pulse shaping in OFDM. 5
d) Differentiate between IS-95 and CDMA-2000 system 5

Q.2 a) Explain the architecture of GSM system with the help of block diagram. Explain various interfaces existing between different subsystems. 10
b) Explain in detail CDMA-2000 layered structure with the help of block diagram. 10

Q.3 a) With the help of block diagram explain forward IS-95 CDMA system. 10
b) With a schematic, explain DSSS transmitter and receiver. What is the need of spreading the sequence ? 10

Q.4 a) Explain OFDM block diagram and derive the equation for OFDM signal. 10
b) Explain the need of power control in CDMA. Explain the methods of power control implemented in CDMA IS-95 system. 10

Q. 5 a) Explain different traffic and control channels in GSM for mobile communication. 10
b) Explain in detail various methods to improve coverage and capacity in mobile communication. 10

Q. 6 a) What is the need of RAKE receiver. Explain the working of RAKE receiver with schematic block diagram. 10
b) A 30 MHz total spectrum is allocated for wireless duplex cellular system and each simplex channel has 30 KHz RF bandwidth. Find 10
i) No. of duplex channels available.
ii) No. of channels per site if N=4 and N=7 frequency reuse is implemented.

Q.7 Write short notes on:
a) Bluetooth Network 6
b) Frame structure of GSM 7
c) Data services in CDMA-2000 system. 7

B.E sem VII OLD

Filter Design ETRX

QP Code : 2160

(3 Hours) [Total Marks : 100

N.B. : (1) Question No.1 is **compulsory**.
(2) Attempt any **four** from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. Attempt the any **four** from the following :— 20
   (a) Design steps for Impulse Invariant method for IIR filter.
   (b) State the concept of adaptive filter.
   (c) Explain MMSE criteria
   (d) Compare FIR and IIR filter.
   (e) Why antialiasing filter is required ?
   (f) What is inductance simulation ?

2. (a) Discuss the effect of decimation and interpolation in time and frequency domain with suitable example. 10
   (b) Apply BLT to $H(s) = \frac{2}{(s+1)(s+2)}$ with T = 1 sec and find H(z). 10

3. (a) Explain the design steps of FIR filter using frequency sampling technique. 10
   (b) Explain Gibb's Phenomenon. State its significance in FIR filter design 10

4. (a) Determine the order and poles of lowpass Butterworth filter that has 3dB attenuation at 500 Hz and an attenuation of 40 dB at 1000 Hz. 10
   (b) Explain frequency warping effect in BLT. 10

5. (a) Describe Leap Frog realization technique in detail. 10
   (b) Design filter with 10

$$Hd = e^{-j3w} \quad \text{for } -\frac{\pi}{4} \le w \le \frac{\pi}{4}$$

$$= 0 \quad \text{for } \frac{\pi}{4} \le w \le \pi$$

Using Hamming window with N = 7

6. (a) What is FDNR ? State its properties. 10
   (b) Explain LMS and RLS algorithms in detail. 10

7. Write short note on any **four** :— 20
   (a) Matched Z transform
   (b) Subband coding
   (c) Principle of switched capacitor filter
   (d) Working principle of Weiner filter
   (e) Explain quadrature mirror filtering in multirate DSP.

———v———