B.E sem VII Rev.2012 CBSGS NOV-2016 21-12-16

Sub:- ASIC Verification.

ETRX

Q. P. Code : 728901

Time:-3 Hrs **Marks: 80**

N.B. : 1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve the following (Any Four) **20 Marks**

A. Highlight the important features of Spartan -6 family devices.

B. What are semaphore and describe their use in SystemVerilog with suitable example.

C. Create a C function that prints out C: Hello World and Create a SystemVerilog module that calls the C function.

D. Describe the difference between code coverage and functional coverage. Which is more important and why we need them.

E. Enumerate the differences between rand and randc with suitable examples.

Q2. A. Give comparison of verification technology options. **05 Marks**

B. Create the SystemVerilog Code with the following requirements: **05 Marks**

I. Create a 512 location integer array
II. Create a 9-bit address variable to index into the array
III. Initialize the last location of the array to 5
IV. Call a task, my_task(), and pass it the array and the address
V. Create my_task() that takes two inputs, a constant 512-element integer array passed by reference, and a 9-bit address. The task calls a function, print_int(), and passes the array element, indexed by the address, to the function, pre-decrementing the address.
VI. Create print_int() that prints out the simulation time and the value of the input. The function has no return value.

C. Write the SystemVerilog code for the following items: **05 Marks**
1) Create a class ***Exercise1*** containing two variables, 8-bit ***data*** and 4-bit ***address***. Create a constraint block that keeps ***address*** to 3 or 4.
2) In an ***initial*** block, construct an ***Exercise1*** object and randomize it. Check the status from randomization.

D. Explain the concept of switch level modeling and how it is done in verilog. Write switch level code for CMOS inverter in verilog. **05 Marks**

[TURN OVER]

Q3. A. What is necessity of clocking block and give detail explanation of clocking block with suitable example. **05 Marks**

B. Which are sequential control statements? Give one suitable example of each. **05 Marks**

C. Explain about the Timeunit, Timeprecision and timescale. **05 Marks**

D. What are different randomization built-in methods? Explain them with suitable examples. **05 Marks**

Q4. A. Explain various fork statements supported in systemverilog. **05 Marks**

B. With respect to SystemVerilog explain the following with suitable example **05 Marks**

I. Abstract classes

II. Parameterized classes

C. For the following code determine the order and time of execution for each statement if a join or join_none or join_any is used. The order and time of execution between the fork and join/join_none/join_ any is the same, only the order and execution time of the statements after the join are different. **05 Marks**

```
initial begin
  $display("@%0t: start fork...join_none example", $time);
  fork
        begin
          #20 $display("@%0t: sequential A after #20", $time);
          #20 $display("@%0t: sequential B after #20", $time);
        end
        $display("@%0t: parallel start", $time);
        #50 $display("@%0t: parallel after #50", $time);
        begin
          #30 $display("@%0t: sequential after #30", $time);
          #10 $display("@%0t: sequential after #10", $time);
        end
  join or join_any or join_none
  $display("@%0t: after join", $time);
  #80 $display("@%0t: finish after #80", $time);
end
```

D. Create a class called **MemTrans** that contains the following members, then construct a **MemTrans** object in an **initial** block **05 Marks**

i. An 8-bit **data_in** of logic type

ii. A 4-bit **address** of logic type

iii. A void function that **print** out the value of **data_in** and **address**

iv. Create a custom constructor, the **new** function, so that **data_in** and **address** are both initialized to 0.

Q5. A. For the code below, write a covergroup to collect coverage on the test plan requirement: "All ALU opcodes must be tested". Assume the opcodes are valid on the positive edge of signal *clk*. **05 Marks**

```
typedef enum {ADD, SUB, MULT, DIV} opcode_e;

class Transaction;
  rand opcode_e opcode;
  rand byte operand1;
  rand byte operand2;
endclass
Transaction tr;
```

B. Where and how are assertions used? **05 Marks**

C. Explain how built-in method randomize() can be used as checker. **05 Marks**

D. Given the following code, determine what will be displayed. **05 Marks**

```
`default_nettype none
module test;
string students[$] = {"Amit", "Mohit", "Rohit"};
initial begin
  $display("Students[1] = %s", students[1]);
  students.insert(2, "Patil");
  $display("Students[2] = %s", students[2]);
  students.push_front("Ajay");
  $display("Students[2] = %s", students[2]);
  $display("pop_back = %s", students.pop_back);
  $display("students.size = %d", students.size);
end
endmodule // test
```

Q6. A. List and explain various coverage methods provided in SystemVerilog. **05 Marks**

B. Explain the following with suitable example
   a. Conditional coverage
   b. Branch coverage **05 Marks**

C. With suitable example for each, explain the following with respect to Sequences in assertions:
   a. Constant Range Delay
   b. Nonconsecutive Repetition
   c. Sequence And
   d. Sequence Or
   e. Sequence Within **05 Marks**

D. Explain the layers of DPI-C. **05 Marks**

B.E. Sem VII Rev. 2012 CBSGS NID-2016

Subj.- Artificial Intelligence. Dt: 21/12/201

ETRX

QP Code : 728801

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question no. **1** is **compulsory**
(2) Solve any three from the remaining five questions
(3) Assume suitable data if necessary.
(4) **Figures** to the **right indicate** full **marks.**

1. Attempt **any four** from the following questions **20**
   (a) Draw a simple artificial neuron and discuss the calculation of the output. State any two characteristics of an artificial neural network.
   (b) Indicate the differences between excitatory and inhibitory weighted interconnections.
   (c) Compare and contrast BAM and Hopfield networks.
   (d) Explain fuzzification and defuzzification process.
   (e) Explain the difference between supervised and unsupervised learning.

2. (a) Draw the model of Adaline network. Explain the training algorithm used here. **10**
   (b) What are linearly separable and nonseparable pattern classes? Discuss how perceptrons can be used to classify each of them. **10**

3. (a) What are the two types of discrete Hopfield nets? Draw the architecture of discrete Hopfield net. State the testing algorithm used in discrete Hopfield Network. **10**
   (b) Draw a simple neural network with a single neuron, four input points and one output point. Apply Hebbian rule to this network with binary activation function and obtain the updated weight vector. The initial weight vector is $W^t = [1\ -1\ 0\ 0.5]^t$ and the training set consists of three inputs, $X_1 = [1\ -2\ \ 1.5\ 0\ ]^t$; $X_2 = [1\ -0.5\ -2\ -1.5]^t$; $X_3 = [0\ 1\ -1\ \ 1.5]^t$ Assume learning constant as 1. **10**

4. (a) What are LVQs? Explain LVQ1 algorithm in detail. **10**
   (b) With a neat architecture, explain the training algorithm of Kohonen self-organizing feature maps. **10**

5. (a) Three fuzzy sets are defined as: **10**

$$\underset{\sim}{A} = \left\{\frac{0.1}{30} + \frac{0.2}{60} + \frac{0.3}{90} + \frac{0.4}{120}\right\}$$

[TURN OVER]

$$\underset{\sim}{B}=\left\{\frac{1}{1}+\frac{0.2}{2}+\frac{0.5}{3}+\frac{0.7}{4}+\frac{0.3}{5}+\frac{0}{6}\right\}$$

$$\underset{\sim}{C}=\left\{\frac{0.33}{100}+\frac{0.65}{200}+\frac{0.92}{300}+\frac{0.21}{400}\right\}$$

Find the following:

(a) $\underset{\sim}{R}=\underset{\sim}{A}\ X\ \underset{\sim}{B}$

(b) $\underset{\sim}{S}=\underset{\sim}{B}\ X\ \underset{\sim}{C}$

(c) $\underset{\sim}{T}=\underset{\sim}{R}o\ \underset{\sim}{S}$ using max-min composition

(d) $\underset{\sim}{T}=\underset{\sim}{R}o\ \underset{\sim}{S}$ using max-product composition

(b) Explain any four defuzzification methods with suitable diagrams. **10**

6. Write short notes on **any four**: **20**

(a) Types of activation functions

(b) Properties of neural networks

(c) Boltzmann Machine

(d) Rate of learning

(e) ANFIS

BE Electronics Sem-VII (CBGS) 15/12/2016
Computer Comm. Network

Q.P. Code : 728602

(3 hours) [Total marks: 80]

N.B: (1) Answer any four questions out of six questions
(2) Question No:1 is compulsory
(3) Assume suitable data if necessary

1. Answer any four questions briefly: (20)
   a) Explain PPP header format.
   b) Compare TCP and UDP.
   c) List the categories of UTP cables. How is noise interference minimized in twisted pair cables?
   d) Distinguish between OSPF and BGP.
   e) What is sub netting? List advantages and disadvantages of the same.

2. a) List and explain different ARQ techniques. Specify the maximum window size for each with justification. (10)
   b) What is piggybacking? Give an example of Piggybacked frame. (10)
   Sketch the appropriate HDLC frames for the following scenario involving Primary station 'A' and two Secondary stations B and C:
   i. Primary station A wishes to establish a Normal Response mode link with Secondary stations B and C.
   ii. Both the stations B and C send positive acknowledgements to A.
   iii. Station A sends a polling command to B and B sends 4 data frames. The third frame is lost during transmission.
   iv. Assuming Selective repeat ARQ, station A sends negative acknowledgement to station B.
   v. Station B resends the frame and A sends positive acknowledgement.
   vi. Station A now polls station C and station C responds with ready response. A sends three data frames to C and C sends positive acknowledgement to indicate the receipt of error free data frames.

3. a) Differentiate between IPv4 and IPv6. (10)
   Determine the class and network address for the following IP addresses (Assuming subnetting is not being used and use default mask)
   i) 84.42.58.11 ii) 195.38.14.13 iii) 144.62.12.9
   b) What is meant by 'blocking' in circuit switching networks? Bring out the advantages of multi stage space division switching over single stage switching. (04)
   c) Sketch three stage space division switch for N=15, n=5 and k=2 (06)
   What is the condition required to make it non blocking?
   For the same specifications, sketch three stage TST switch using TSI modules.

[TURN OVER]

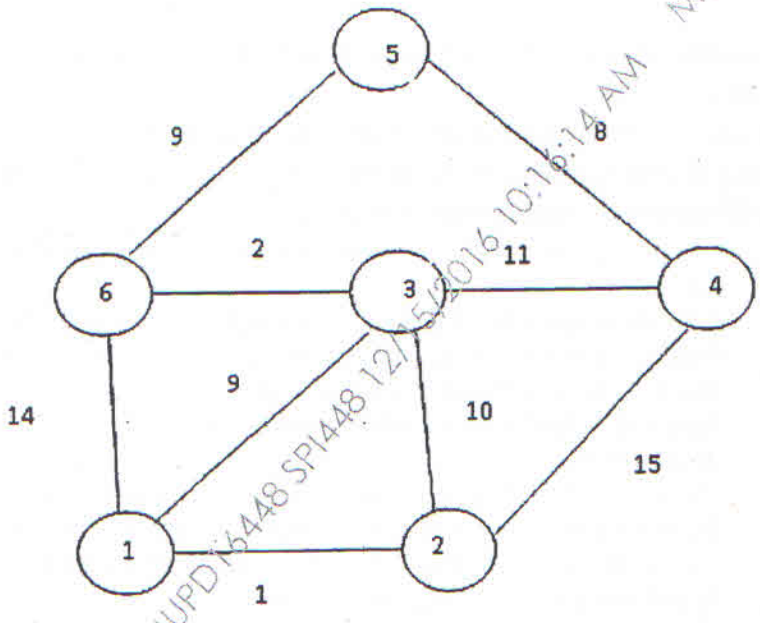
4. a) Draw OSI reference model and explain function of each layer. Name the layers responsible for: i) end to end reliability ii) link to link reliability. (10)

   b) Define the utilization or efficiency of the line and derive the expression for stop and wait flow control. Calculate the maximum link utilization for the following cases: (10)

   i) Stop and wait flow control
   ii) Sliding window flow control with window sizes of 4 and 7

   Link specifications:
   Frame length= 1000 bits/frame
   Velocity of propagation = 2×10^8 m/sec
   Link distance= 20km
   Data rate= 20 Mbps

5. a) Apply Dijkstra's and Bellman Ford algorithm to the given network and find the least cost path between source node 1 to all other nodes: (10)



   b) Draw and explain TCP header format with the help of a neat diagram. (10)

6. Write short note on: (Any TWO) (20)

   a) Congestion control techniques
   b) ADSL
   c) TCP connection establishment and release
   d) CSMA/CD

Sem-VII Electronics. (CBGS) 8/12/16

Power Electronics-II

QP Code : 728502

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question No. **1** is **compulsory**.
(2) Answer any **three** questions from remaining five questions.
(3) Assume suitable **data** where ever **necessary**.

1. Solve any **four** questions :— **20**
   (a) Differentiate between Plugging and generating mode in AC Motor.
   (b) With the heip of diagram explain principle of working of induction heating.
   (c) For a single phase full converter with inductive load, if the source inductance Ls is considered find the average output voltage and reduction in the average output voltage due to overlap if α = 30 deg. and μ=2 deg. with supply voltage of 230 volts.
   (d) The speed of 10 HP separately excited DC motor is controlled by single phase full converter. The rated armature current is 30 A. Ra = 0.5 ohm. The ac supply voltage is 260 volts. The motor voltage constant is 0.182V/rpm. While in motoring action with back emf of 192 volts the polarity of it is reversed for regenerative action. Calculate firing angle to keep the motor current at its rated value.
   (e) Explain battery charging circuit in detail.

2. (a) Explain stator voltage control technique for three phase induction motor. Draw torque-slip characteristics. **10**
   (b) Explain three phase fully controlled bridge converter with source inductance. Draw waveforms. **10**

3. (a) Draw and explain average model and state space model for buck DC-DC converter in detail. **10**
   (b) What is the need of SVM, Explain SV sequence and SV switching in detail in space vector modulation. **10**

4. (a) Explain continuous mode fly-back converter in continuous mode. Derive the relation for load voltage **10**
   (b) A 3 phase 4 pole induction motor is operated from 415V / 50 Hz supply. Stator voltage control technique is to be applied to vary the speed. The motor is driving a load torque of 100 N-m. Find out the following if motor speed is 100 rad/sec. i)Slip ii)P_{ag} iii) P_{slip} iv) P_{mech} v) The efficiency of rotor circuit. **10**

[TURN OVER

5. (a) Draw and explain semi converter drive for separately excited DC motor. Draw torque-speed characteristics. **10**

(b) State and explain different characteristics of battery. **5**

(c) A UPS driving 600 W load which has a power factor of 0.8. The efficiency of the inverter is 80 percent. The battery voltage is 24 volts dc. Assume that there is a separate charger for the battery. Determine the followings. i) KVA rating of the inverter ii) Wattage of the rectifier. **5**

6. Write short notes on the following :— **20**

(a) On line and off-line UPS

(b) Controllers in DC-DC converters

(c) Torque-slip/speed characteristics of induction motor with operating regions with different value of slip.

Sem VII ETRX Embedded System Design 24 Nov 2016

CBCGS

QP CODE : 631400

(3 Hours) (Total Marks : 80)

N.B. Question no. 1 is compulsory.
All questions carry same weightage/marks.
Attemt any other 3 from remaining 5 questions. Attempt total 4 questions
Assume suitable date whereever necessary.

Q1.a. What are' the challenges while meeting low power consumption, performance, low-cost requirement for an embeded system. Explain how they affect other? (5)
b. What kind of communication an embedded system may need? Describe any two types (5)
c. Why C programing is popular for embedded programing? Describe related features. (5)
d. Cortex-A8, R4, M3 are suitable for certain class of applications, justify how? (5)

Q2.a. What features of cortx-M3 makes it suitable for low-power, RTOS based applications. (10)
b. What is CAN protocol? Describe topology and Frame formats with significance of fields. (10)

Q3.a. What is need of debug and trace facility? How cortex-M3 supports it? (10)
b. For low power design which microcontroller architecture will you use? Why? What is typical design strategy for achieving low-power consumption. (10)

Q4.Heart is having a natural pulse generator which is responsible to rythmically beating of heart. Malfunctioning of that leads to arythmic heart beating. Design a pacemaker (pulse generator) which generates electrical pulses to trigger heart, if it senses irregular(or low) heart rate. This pacemaker is typically inplanted inside body near chest. Assume appropriate design challenge and design an embeded system (pacemaker) which can sense and trigger (if required) heart to bring heart back to normal rythmic beating. For this design develop
a. Functional model /FSM which describes functioning of system
b. Hardware block diagram which describes typical hardware building blocks
c. Software architecture which describe typical functions/drivers/tasks required in program d. piscuss special design challenges for this design and suggest solutions/approach
e. Suggest list of components with justification. (20)

Q5.a. What is Real time operating system's role, function in an embeded system? Describe various uCOS-II c-functions which are used to implements RTOS functions/role. (10)
b. What is shared data? How it is handled in RTOS? What are priorty inversion problems? How priority inversion problem can be addressed/solved? (10)

Q6.Write short notes on any four.
a. Task scheduling policies (any three) and its impact on average waiting, turn-around time
b. Compare FPGA/CPLD based embedded system against Microcontroller based
c. Testing methodologies, tools and need.
d. Wireless embedded communication.
e. Inter process communication in RTOS (20)

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Sem VII CBGS Etrx IC Tech.

Q.P. Code : 728402 01/12/16

(3 Hours) [Total Marks : 80

N.B. 1) Question No. 1 is compulsory
2) Solve any three questions from the remaining questions
3) Assume suitable data if necessary

1. Solve any four of the following. (5 marks each) (20)
   (a) Explain various charges in the gate oxide after fabrication of MOSFET.
   (b) What is Trench Isolation? Explain its use in VLSI technology.
   (c) Classify crystal structure with respect to resistivity and periodicity of atoms.
   (d) Enlist the steps for obtaining Silicon from Sand.
   (e) Explain Molecular Beam Epitaxy.

2. (a) Define Range, Projected Range and straggle with respect to Ion Implantation. Also explain the damage produced due to light ion and heavy ion with neat diagram. (10)
   (b) Describe APCVD process with neat diagram. Why wafers are lying horizontal in this process. Enlist drawbacks of this process. (10)

3. (a) List out common Unit processes in IC Fabrication. What is the difference between N-well and P-well process? Draw final cross-sectional view of CMOS inverter fabrication using N-well process with appropriate labels? (10)
   (b) Draw layout of CMOS inverter along with its circuit diagram. Mention clearly all dimensions as per lambda rules. Explain buried and butting contact. (10)

4. (a) Explain Steps of Lithography with suitable diagrams. Also classify Lithography techniques. (10)
   (b) What is SOI technology? Enlist methods for fabrication of SOI. Explain any one of it. (10)

5. (a) Describe with the help of a neat diagram Hayness-Schokley experiment for measurement of Drift Mobility of n-type semiconductor. (10)
   (b) Compare evaporation and sputtering methods for metal deposition. Which methods are commonly used for deposition of Silicon, SiO_2 and metals? (10)

6. Write short notes on any four of the following. (5 marks each) (20)
   (a) Parametric test and functionality test for IC testing
   (b) Electric package reliability.
   (c) Silicon Crystal defects
   (d) Multiagte device Structures
   (e) MESFET fabrication process