TE Sem VI (Electronics) CBGS
Power Electronics

14/12/2016

QP Code :591901

(3 Hours) **[Total Marks :80**

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any **three** questions out of remaining questions.
(3) **Assume** suitable **data** wherever **necessary.**

1. Solve any **four**. **20**
   (a) Explain dynamic characteristics of SCR
   (b) Compare IGBT and Power BJT
   (c) What is need of free wheeling diode in rectifiers with example.
   (d) Draw and explain DIAC characteristics
   (e) What is the need of thyristors in Electronic Circuits?

2. (a) Draw and explain full controlled rectifier with R-L load .Draw waveforms when a = 60° **10**
   (b) Explain working of step up Chopper with proper waveforms. **10**

3 (a) A single phase half bridge inverter has resistive load of 8 ohms and DC input voltage Edc=50V Calculate: **10**
   (i) RMS output Voltage
   (ii) Average and Peak current of each Thyristor
   (iii) Output Power Po
   (b) Explain voltage control technique in Inverter using sinusoidal PWM method **10**

4. (a) Explain dual converter with proper waveforms **10**
   (b) Explain working of three phase bridge Inverter. **10**

5. (a) Explain Power MOSFET construction and characteristics. Give one application **10**
   (b) Design relaxation oscillator circuit for SCR using UJT for following data: **10**
   $\eta = 0.71, Ip = 0.5mA, Vp = 16V, Iv = 2.5mA, Rbb = 5.5K\Omega$. with emitter open.
   The firing frequency is 3KHz, C=0.047 μF

6. Write short notes on:- **20**
   (a) Buck-Boost mode regulator
   (b) Protection circuits for SCR
   (c) Cyclo-converters and applications
   (d) Forced commutation in SCR

Sem-VI (Electronics) (CBSGS) 7/12/16.

Computer Organization.

Q.P. Code : 591802

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is **compulsory**.
(2) Attempt **any Three** questions from remaining **questions**.
(3) **All** questions carry **equal marks**.
(4) **Figures** to the **right** indicate **full marks**.

1. (a) Calculate the effective memory access time for **20**
M1: 50 ns access time,
M2: 400 ns access time and hit ratio of M1 : 0.95
(b) Explain nano-programming and enumerate is advantages.
(c) Explain the principles of locality of reference used in cache memories.
(d) Show the address decoding for 128KB ROM (32 bit memory) using 32 bit addresses.

2. (a) Explain hardwired control unit with a neat diagram. Describe clearly the generation of control signals with examples. **10**
(b) A 32 bit processor has a 32 bit memory address. It has 8KB of cache memory. The computer follows 4-way set-associative mapping with each cache line size being 16 bytes. Show the memory address format and explain the process of lookup. (Draw neat diagrams). **10**

3. (a) Explain the register structure of the IA-32 family with neat diagrams. Describe the functions of each register in brief. **10**
(b) Explain the paging mechanism. State advantages of paging and the importance of the Translation Look aside Buffer (TLB) in paging. **10**

4. (a) Compare CISC and RISC design philosophies in detail (atleast five points of difference). **10**
(b) State the advantages of pipelining. Explain various types of pipeline hazards and their solutions. Give examples. **10**

5. (a) Explain the multi-bus data path organization with a neat diagram. **10**
(b) Write a control sequence and explain the steps for the following instruction **10**
ADD R2, [R1]

6. Write short notes on : **20**
(a) Cache coherency
(b) Storage devices
(c) Flynn's classification

20/12/2016

T.E Sem VI (CBGS)
(ETRX)
DSP.

Q.P. Code : 592001

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question number **1** is **Compulsory**.
(2) Solve any **three** question out of remaining
(3) Assume suitable data if required.

1. Answer any **four**
   (a) Differntiate between Butterworth and chebyshev filter **5**
   (b) Explain the concept of pipelining in DSP processor **5**
   (c) Expalin frequency warping effect in designing IIR filter using BLT method. **5**
   (d) Explain Quantization effect in computation of DFT **5**
   (e) State the relationship between DFS, DFT and Z Transform **5**

2. (a) Compute IDFT of the following sequence using inverse FFT algorithm. **10**
   x (k) = {3,0,3,0,3,0,3,0}
   (b) Prove the Parseval's theorem for the sequence x(n) = {2,4,2,4} **5**
   (c) Find the linear convolution and circular convolution of the sequences x(n) = {1,2,1,2} and h(n) = {4,0,4,0} **5**

3. (a) Design an analog Butterworth filter that has - 2dB passband attenuation at frequency of 20 rad/sec and atleast -10dB stopband attenuation at 30 rad/sec. **10**
   (b) Convert the following filters with system functions **10**

   (i) $H(s)=\frac{1}{(s+2)(s+0.6)}$

   (ii) $H(s)=\frac{(s+0.1)}{(s+0.1)^2+9}$

   into a digital filter by means of impulse invariant and BLT method.

4. (a) Explain the concept of linear phase in FIR filter. **10**
   prove the following statement 'a filter is said to have linear phase response if its phase response is $\theta(w) = -\alpha w$.
   (b) Design a low pass FIR filter with 7 coefficients for the following specifications passband frequency = 0.25 khz and sampling frequency = 1 khz. Use hamming window in designing. **10**

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5. (a) Draw neat architecture of TMS 320C67xx DSP processor and explain each block. **10**

   (b) Explain addressing modes of DSP processor with example. **10**

6. Write short notes on:- (any **three**) **20**

   (a) Subband coding

   (b) Application of DSP processor to Radar signal processing

   (c) Limit cycle oscillations

   (d) Product quantization error and input quantization error

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