Sem-VI EXTC (CBGS) 27/12/2016

VLSI Design.

Q.P. Code : 588804

Time: 3 Hrs **Marks: 80**

N.B. :
1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve any **Four** of the following **20 Marks**

A. Draw layout for 2 input CMOS NAND gate.

B. How to distribute a clock properly in VLSI chip?

C. Draw layout for minimum size 6T SRAM cell.

D. Explain the issues associated with pass transistor logic with suitable example.

E. Explain constant voltage scaling?

Q2. A. Explain the fabrication process flow for NMOS with proper device cross section and layout. **10 Marks**

B. Explain pseudo NMOS logic with suitable example. **05 Marks**

C. Show realization of MOSFET based one Bit Shift Register,. **05 Marks**

Q3. A. Design the circuit and draw layout for the function $Y = \overline{(D + E + A)(B + C)}$ using CMOS logic. Also find equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $(W/L)_P=30$ for all PMOS transistors and $(W/L)_n=10$ for all NMOS transistors. **10 Marks**

B. What are the problems of Domino logic? Also suggest remedy for these problems. **10 Marks**

Q4. A. With neat diagrams explain the principle of working of NOR flash. **10 Marks**

B. Draw and explain Barrel shifter. **06 Marks**

C. Draw schematic and layout for 4:2 decoder. **04 Marks**

Q5. A. Explain ripple carry adder in detail. **10 Marks**

B. Explain how to ensure faithful write operation in case of 6T SRAM Cell. **06 Marks**

C. Compare LEVEL 1 and LEVEL 2 MOSFET model. **04 Marks**

Q6. A. With suitable diagrams explain on chip clock generation circuit. **05 Marks**

B. Explain a typical power distribution scheme followed in VLSI chip. **05 Marks**

C. Describe the dynamic power dissipation in CMOS. **05 Marks**

D. Explain Latch-up in CMOS. **05 Marks**
