M.E. sem I Etrx, Microprocessor and systems-I. 22/5/08

ws April 08 468

Con. 3076–08.

BB–4609

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Assume **suitable** data if **necessary** and state the assumptions **clearly**.

1. Design a SBC with the following specs. **20**
   CPU : 80386 dx operates at 16 MHz
   ROM : 256 KB EPROM using 32 KB devices
   RAM : 1 GB SRAM using 1 GB device.
   I/O : Interrupt drivers, 2 input and 2 output ports
   Draw a neat diagram show memory and I/O maps and decoding logic used.

2. Explain Trojan Horse attack. How operating system can prevent such an attack using ARPL instructions ? **20**

3. Draw a neat diagram and explain the various functional units of 80386 DX processor. Highlight the control and debug registers. **20**

4. (a) '80386 DX is all ideal processor for embedded system applications'. Justify your answer with suitable diagram. **10**
   (b) Discuss the I/O protections of 80386 DX processor. **10**

5. (a) Explain with neat diagram the use of ISA bus with 80386 dx to handle 32 bit data operation. **10**
   (b) Explain the ISA timer. **10**

6. (a) What is the necessity of cache subsystem ? Explain the following terms : **10**
      (i) Cache coherancy
      (ii) Buffered write through
      (iii) Snooping and suarfing
   (b) Design a 2–way set associative as well as direct map cache organisation for the following specification :– **10**
   Mains memory 4 MB, cache memory 16 KB with line size = 4 bytes.
   Give the directory entry for both in details .

7. (a) Develop an ISA based data acquisition card for one analog input and one analog output. **8**
   (b) How double faults are handled in 80386 protected mode ? **6**
   (c) Discuss interrupt structure of 80386 EX and interrupt configuration register. **6**
