M.E. Sem II
VT-May,08 86 Etrx VLSI Design 23/5/08

Con. 3116–08. BB–4729

(3 Hours) [Total Marks : 100

N.B.:- 1) Question No1 is compulsory.
2) Attempt any four out of the remaining six questions.
3) Assume any suitable data wherever required and justify the same.
4) Figure to the right indicates marks.

Q1. a) Explain flat condition for MOS Capacitor, also explain band bending in case of accumulation, depletion and inversion mode 05

b) What are different factors on which threshold voltage depends 05

c) A CMOS inverter has $\mu_n = 2.5\mu_p$ How you can make Fall time same as Rise time? 05

d) Determine the oxide thickness if the constants A=0.05μm/s and B=0.72 $\mu m/s^2$ for i) short time, t =0.01h ii) long time, t = 100h. 05

Q2. a) Implement following function 10

$F = A.(B+C).(D+E)$

Draw Stick diagram and Layout for the same.

b) Find the Threshold shift due to the body effect 10

Where VSB = 3 Volts

$N_A = 3 \times 10^{16}\ cm^{-3}$, $t_{ox} = 300^0 A$, $\varepsilon_o = .8.85 \times 10^{-14}$ F/cm

$\varepsilon_{ox} = 3.9\ \varepsilon_{o,\ si} = 11.7\ \varepsilon_o$ $ni = 3 \times 10^{10}\ cm^{-3}$ $q = 1.6 \times 10^{-19}$C

Q3. a) What is the need of Scaling? Explain limitations of scaling. State different types of the same and compare their effects. 10

b) Describe with neat diagram various steps involved in fabrication and sketch each mask steps in cross-sectional view of wafer for CMOS Inverter. 10

Q4. a) Derive expression for drain current in nMOS device in linear region of operation and then derive the current in saturation region from the previous expression. 10

b) Explain following short channel effects: 10
i) DIBL
ii) Drainpunchthrough
iii) Hot electron effect
iv) Velocity Saturation

Q5. a) Draw the transfer characteristics for CMOS inveter. and derive expression for output voltage in region B. 10

b) What do you mean by Supper-buffer? Explain Inverting and noninverting type of supperbuffer. Also suggest alternatives for supper buffer. 10

Q6. a) Explain different logics such as: Precharge-Evaluation logic Domino Logic and Zipper logic .Explain their significances. 10

b) Explain what is the significance of Design Rules? State Mead-Conway Rules for different layers in VLSI Technology. 10

Q7. Write Short notes on (Any Four) : 20

a) Ion Implantation
b) Photolithography
c) Twin Tub Method
d) Burried and Butted Contact
e) CMOS Testing.