7/6/2011

Karu-upq Ki-11 121

B.E ETRX VIII (Rev)
Embedded System & real Time Programming

Con. 3893–11. **(REVISED COURSE)** **RK–4632**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** from the remaining **six** questions.

1. (a) Suggest various techniques used for inter process communication in an embedded system with relevant examples. Also, explain strategies used for synchronization between processes. 15
   (b) With the help of a neat diagram, explain the different states a task can be in and the transitions between them. 5

2. (a) Explain the various operating modes of the ARMY processor. 10
   (b) What is the Shard Data Problem ? Explain various techniques to overcome it. (With relevant examples). 10

3. (a) Explain the interface of Alphanumeric LCD with any microcontroller of your choice. (Draw neat diagram) 7
   (b) Write a detailed note on the CAN Bus explaining its features and protocol. 7
   (c) Differentiate between CISC and RISC processors. 6

4. (a) What is interrupt latency in Embedded systems ? Suggest methods to reduce latency. 10
   (b) Explain what is the Linear sequential model in Embedded software development. 10

5. (a) Explain the Register set of the MSPHZO RISC controller (working Registers, SFRs, status Register etc.) 10
   (b) Write a detailed note on the THUMB mode of operation of the ARMY processor. 10

6. (a) Explain Bounded and unbanded priority Inversion problem. Suggest methods to overcome / minimise it. 10
   (b) Explain the various program modelling techniques used in Embedded system design. 10

7. Write short notes on :— 20
   (a) Watching Timer
   (b) Serial Peripheral Interface (SPI)
   (c) Different types of memories in Embedded systems
   (d) Digital Signal Controllers (DSCs).

B.E ETRX VIII (Rev)
Elective II: Advanced Networking Technologies

Con. 3958-11. (REVISED COURSE) RK-4642

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is **compulsory**.
(2) Solve any **four** from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data wherever **necessary**.

Q.1 A) How do the layers of TCP/IP model correlate to the layers of OSI model? (5)

B) Distinguish between the ATM and frame relay. (5)

C) Explain in brief the various security threats. (5)

D) With the help of a neat sketch explain DWDM. (5)

Q.2 A) Compare and contrast Ubiquitous and Hierarchical access. (10)

B) Explain subnetting and supernetting. (10)

Q.3 A) Sketch the frame format of frame relay and explain address field. How it provides congestion control and quality of service. (10)

B) What do you mean by access layer design? explain. (10)

Q.4 A) Explain in detail Repeaters, Routers, Bridges and Switches. (10)

B) Give the SONET/SDH hierarchy in brief. (5)

C) With a suitable sketch, explain ATM cell format for user-network interface. (5)

Q.5 A) Explain ATM adaptation layer also describe the concept of VPI and VCI. (10)

B) What is remote monitoring? Explain benefits of remote monitoring. (5)

C) Write a short note on SONET hardware. (5)

Q.6 A) Discuss designing a network management solution. (10)

B) Describe network security safeguards in detail. (10)

Q.7 Write short notes on : (20)

A) IEEE 802.11

B) Internetworking protocols

C) OAM & P

D) Enterprise Network Security

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B E ETRX VIII (Rev)
Elective II - DSP Processors & Architectures

Con. 3983-11. (REVISED COURSE) RK-4635

(3 Hours) [Total Marks : 100

N.B. 1 Question No. 1 is compulsory.
2 Out of the remaining questions attempt any 4 questions.
3 All questions carry equal marks.

Q1

With respect to programmable digital signal processors in general, write a comprehensive note on the architectural features covering the points of bus and memory structure, MAC unit, pipelining feature, multi-ported memories etc. (20)

Q2

a) With a neat block diagram explain the architecture of TMS320C5X processor. Highlight the functions of central arithmetic logic unit (CALU) and auxiliary register ALU (ARAU). (14)
b) List the on-chip peripherals and their functions in TMS320C5X processor. (06)

Q3

a) With the help of examples explain the various addressing modes of C5X processor (14)
b) Explain briefly the addition and subtraction instructions in C5X processor. (06)

Q4

a) Explain the architectural features of ADSP 21xx series of digital signal processors. Compare the same with those of TMS320C5X series. (14)
b) How does the clock (crystal) speed affect the system through-put in a typical controller based system? What are the techniques used by designers to retain high through-put at lower crystal speeds for reducing EMI. (06)

Q5

a) Discuss the architectural features of TMS320C6X digital signal processor and compare the same with DSP563XX from Motorola. (14)
b) What is the need for high speed, high resolution ADC and DAC in digital signal processors along-with switched capacitor filters? (06)

Q6

a) Write a detailed note on the pipelining operation in C5X series of digital signal processors, with the help of illustrative instruction examples. (14)
b) List the on-chip peripherals and their functional requirements in C5X series of digital signal processors. (06)

Q7 Write short notes on: (20)
a) FFT algorithm using a typical DSP.
b) Implementation of FIR/IIR filters on a DSP.

BE ETRX VIII (Rev)
Robotics & automation

Con. 3840–11. (REVISED COURSE) RK–4629

(3 Hours) [Total Marks : 100

N.B. : 1) 'Question **No. 'One** 'is **compulsory.**
2) Attempt any **'four'** out of remaining **'six'.**
3) Figures to right indicate full marks, **'all'** questions carry equal marks.
4) Assume suitable data wherever necessary.

1, Answer the following questions;

A. Define the following terms : Tool Path, Tool Trajectory, DOF, Precision, Accuracy 05

B. Explain the properties of inverse kinematics solution. 05

C. Define kinematic parameters. What is soft home configuration? 05

D. Draw symbols of Input and Output devices and Switches used in ladder diagrams. 05

2. A. Compare Hard Automation and Soft Automation. State advantages and drawbacks of each. 10

B. Explain the screw transformation. Show that the inverse of a screw transformation is again a screw transformation. 10

3. A. Apply D-H algorithm for SCARA robot and construct a link-coordinate diagram. Compute the arm matrix for the SCARA Robot. 10

B. Define Tool-Configuration vector. Show how to obtain tool roll angle. What are the advantages/disadvantages of Numerical approach and Analytical approach to solve the Inverse kinematics problems? 10

4, A. Explain the shrink and swell operators with an example. How are they applied? List all the properties of these operators. 10

B. Explain the 4 point minimal PNP trajectory for pick and place of objects by using a robot manipulator 10

5. A. What is a GVD? Sketch all the GVD's resulting due to the basic interactions of the obstacles .Derive the necessary equations. 10

B. Explain in details block diagram of PLC(Programmable Logic controller), Hence write ladder diagram programs to Implement Logic functions AND, OR, NOT, NAND, NOR 10

6, A. Obtain Direct kinematics solution of three axis planer articulated robot arm. 10

B. Write specifications of PLC 05

C. Write Industrial Applications of PLC 05

7. Write short notes on **(Any Two)** ; 20

A. Perspective Transformation

B. Workspace Fixtures

C. Template Matching.

BE ETRX - VIII (R) Advance VLSI design L.B

Con. 3263–11. **(REVISED COURSE)** **RK–4644**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.

2) Attempt any four out of remaining six questions.

3) Assume any suitable data wherever required but justify the same.

1. a. Determine intrinsic gate capacitance with 20
t_{ox}= 150A^0, ε_{0x}= 3.9 x8.85x10^{-14} F/cm, and V_G=3.3 Volts
if W=4 μm L=2μm

b. Explain the need of interconnect delay model? Also define Cross-talk in case of VLSI design.

c. Explain the factors on which dynamic power dissipation depends?

d. Explain the parameters to be taken care while design of the adder circuit.

e. Draw the analog design octagon and explain its significance.

2. a. Explain how process variation can cause variation in speed? Explain the concept of Design Corner. 10

b. Draw the schematic of Carry look ahead adder explain how the speed can be improved? 10

3. a. What are the issues of clock distribution? Explain how they are addressed? Also explain how the cross-talk in multilayer system is modeled? 10

b. State the need of Input and Output circuit? Explain with neat diagram the schematic and design consideration for the same. 10

4. a. Implement the following function using NOR-NOR implementation for a PLA 10

i. Y_1=ac+b'c

ii. Y_2= abc+-a'b'c

iii. Y_3=-a'b + ab

b. Explain the clock generation and different types of clocking schemes for VLSI circuit Explain what do you mean by clock skew and clock jitter and how it can be estimated 10

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5. a. Find resistance Rn for nMOS if electron mobility $\mu_n = 560 cm^2/V\text{-sec}$ 10

$t_{ox} = 10$ nm , $\varepsilon_{0x} = 3.9 \times 8.85 \times 10^{-14}$ F/cm , and $V_G = 3.3$ Volts

$V_{THn} = 0.7$ Volts

i) if W=10μm L=0.5μm

ii) if channel width is increased to a value of W=22μm while the channel length remains same.

b. Explain how propagation delay caused by distributed Resistance-Capacitance (RC) in the long wire can be reduced? Derive the expression to neglect the wire-length delay with respect to gate delay 10

6. a. Explain the three knobs on the basis by which CMOS designer optimize the speed of CMOS gate Explain how to approximate calculation of power dissipation at increasing accuracy 10 10

b. State the need and various applications of analog VLSI circuit design. Why analog circuit design is is difficult as compare to digital design?

7. Write a short note on (any four) : 20

a. Charge sharing and transistor sizing.

b. Different clock system

c. The role of sense amplifier

d. Flash cell construction and working

e. Telescopic cascade op-amps

f. Switched capacitor Amplifier

B.E. ETRX - VIII (Rev)
Elective II :- Neural Networks & Fuzzy Systems.

Con. 3771-11. **(REVISED COURSE)** **RK-4638**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Attempt any **four** question out of remaining **six** questions.
(3) **Assumption** made must be **clearly stated.**

1. Solve any **four** of the following :— 20
   (a) Show that any λ-cut relation (for $\lambda > 0$) of a Fuzzy tolerance relation results in a crisp tolerance relation.
   (b) Explain common activation function used in neural network.
   (c) Distinguish between Supervised and Unsupervised Training.
   (d) Compare LMS and Perceptron Learning Laws.
   (e) Explain Delta learning rule.
   (f) What are the salient features of Kohonen's self-organizing learning algorithm ?

2. (a) State and explain the basic learning laws. 10
   (b) Explain perceptron learning rule convergence theorem. Design a perceptron network to implement an AND function, take first input sample [1, 1, 1] 10

3. (a) Derive the back propagation training algorithm for an arbitrary activation function. 8
   (b) How can you approximate a Gaussian function by two sigmoid function ? How can you translate a radial basis function network in to a back propagation network ? 8
   (c) How do we achieve fast learning in ART 2 network ? 4

4. (a) What is the Hopfield model of a neural network ? Explain its algorithm and differentiate between discrete and continuous Hopfield model in terms of energy landscape and stable state. 10

   (b) Two Fuzzy sets $\underset{\sim}{A}$ define on X and $\underset{\sim}{B}$ define on Y 10

$$\underset{\sim}{A} = \left\{\frac{1}{LS} + \frac{0{\cdot}4}{MS} + \frac{0{\cdot}2}{HS}\right\}$$

$$\underset{\sim}{B} = \left\{\frac{1}{SRR} + \frac{0{\cdot}5}{MRR} + \frac{0{\cdot}25}{FRR}\right\}$$

   (i) Find the Fuzzy relation for Cartesian product of $\underset{\sim}{A}$ and $\underset{\sim}{B}$

   (ii) For another Fuzzy set $\underset{\sim}{C}$ define on X

$$\underset{\sim}{C} = \left\{\frac{0{\cdot}1}{LS} + \frac{0{\cdot}3}{MS} + \frac{1}{HS}\right\}$$

   Find relation between $\underset{\sim}{C}$ and $\underset{\sim}{B}$ using Cartesian product.

   (iii) Find $\underset{\sim}{C} \circ \underset{\sim}{R}$ using max-min and max-product composition.

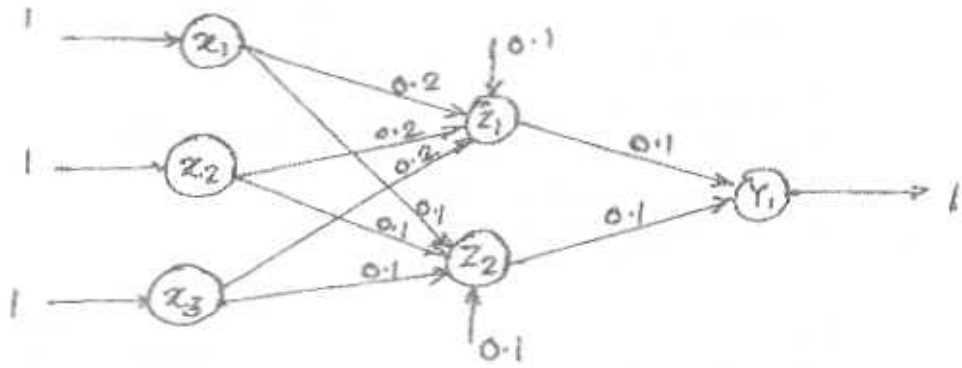
[TURN OVER

5. (a) Show that any λ-cut relation (For $\lambda > 0$) of Fuzzy tolerance relation results in a crisp tolerance relation and any λ-cut relation (for $\lambda > 0$) of a Fuzzy equivalence relation results in a crisp equivalence relation. 10

(b) What is self organizing map ? Explain structure and algorithm of Kohonen self organizing map. 10

6. (a) Explain Brain-state-in-a-box model and explain how it is used for clustering ? 8

(b) For the given network 8



Find new weights when net is presented the input pattern (1, 1, 1) and target output is '1'. Use learning rate of 0·1 and bipolar sigmoidal activation function, the bias is set to '1'.

Activation function : $f(x) = \frac{2}{1+e^{-x}} - 1$ and $f'(x) = 0{\cdot}5\ (1 + f(x))\ (1 - f(x))$

(c) Explain Mc-culloch and pitts model of neuron. 4

7. (a) State and explain various method of defuzzification. 10

(b) Write short notes on the following :— 10

(i) Fuzzy Controller

(ii) Least mean square algorithm.