BE | ETRX | VIII (Rev) 15/5/2012

A. VLSI Design

SA 1st half 131

Con. 3636-12. **(REVISED COURSE)** **GN-7436**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1 is compulsory.**
(2) Attempt any **four** out of remaining **six** questions.
(3) Assume any suitable data whenever required and justify the same.

1. a) Explain metal migration in interconnect. 5
b) Explain programming techniques of EEPROM using hot electron and Fowler-Northeim emission. 5
c) If the width and length of the interconnect is reduced by 30%, then the propagation delay of an interconnect will increase or decrease, by how much %? 5
d) Draw and explain manchester carry out circuit using carry kill bit. Also draw 4-input dynamic Manchester carry chain circuits. 5

2. a) What would be the conductor width of power and ground wires to a50 MHz clock buffer that drives 100 pF of on-chip load to satisfy the metal-migration consideration (J_{AL} = 0.5mA/μm)? What is the ground bounce with chosen conductor size? The module is 500 μm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1ns. (Assume sheet resistance of wire = 0.05Ω/sq). 10
b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. 10

3. a) Give and explain the drawback with ripple carry adder. Explain 4-bit CLA adder with its carry equations, logical network and writs its Verilog description. 10
b) Explain how ESD (electro-static discharge) affect the MOSFET. Give and explain input protection circuits. 10

4. a) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. 10
b) Draw 4 X 4 pseudo-nMOS ROM array circuitry having stored following data. 0011, 1010, 1100, 0101. Also list the no. of address pins, data pins and word lines. 10

5. a) Explain the need of frequency compensation in CMOS operational amplifier. 10
b) Give and explain single phase clock system and explain its drawback. 10

6. a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. 10
b) What is cross talk in IC's? Explain various methods to reduce it. 10

7. Write short notes on (any three): 20
a) Low power design consideration.
b) Reliability issues in CMOS circuits.
c) Carry save adder.
d) Switch capacitor amplifier.

BE | ETRX | VIII (Rev) 19/5/2012
Robotics & Automation

Con. 3833-12. (REVISED COURSE) GN- 7550

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any four questions of remaining six questions.
(3) Assume suitable data wherever necessary.

1) (a)What is fixed and flexible automation 5
(b)Define Kinematic Parameter with the help of suitable diagram. 10
(c)Give any 3 points ,why Inverse Kinematics is Unique ? 5

2) (a)Describe DH algorithm for a 3 DOF articulated Robot .Show all the steps with reference to the figure . 12
(b)Compare and Contrast Direct Kinematics and Inverse Kinematics . 8

3) (a)Find the TCV W(q) for 4-axis cylindrical coordinate robot 12
(b)Define DWE of any robot arm .Explain with their formula 8

4) (a) What is template matching technique of a gray level image and their application to robot vision. 12
(b)What are the moments of an image ?How are the moments use in the shape analysis of objects 8

5) (a)The coordinates of the point 'P' on the body are given by $\{1,2,3\}^T$ 15
Rotate the body about the z-axis by 30^0 and then about the y-axis by 30^0.
Find the new coordinates of the point 'p' w.r.t the fixed frame.
(b)Compare area and Stroke of a Robot, 5

6) (a)Write a PLC ladder logic programme for 4 junction traffic light. 12
(b)Explain the composite rotation matrix (CRM) algorithm. 8

7) (a) Explain PNP motion trajectory in detail . 15
(b)Explain the different types of communication ports used in PLC. 5

BE/ ~~Comp~~ ETRX / VIII (Rev) 24/5/2012
DSP Processors & Architecture

Con. 3977–12. **(REVISED COURSE)** GN–7547

(3 Hours) **[Total Marks : 100**

N.B. : i) Question No. 1 is **compulsory.**

ii) Attempt any **four** Questions from the remaining **six** Questions.

1	a)	Explain how a higher throughput is obtained using VLIW architecture? Give an example of a DSP that has VLIW architecture.	5
	b)	What is the function of interrupt mask register (IMR) and interrupt flag register (IFR) of C5X?	5
	c)	Explain the pipeline operation of TMS320C6X.	5
	d)	Explain the term high memory access bandwidth in relation with P-DSPs. How the same can be obtained in P-DSPs?	5
2	a)	Compare the features of TMS320C5X and TMS320C54XX.	10
	b)	Draw the functional diagram of ARAU unit in C5X and explain the function of various registers/units used in the same.	10
3.	a)	What are the various functional units of C54X CPU. Explain in detail the function of compare, select and store unit (CSSU) and exponent encoder.	10
	b)	What are the on-chip peripherals of C5X DSP?	10
4.	a)	What are the various P-DSP families and their applications? Discuss the various factors to be considered while choosing a DSP Processor.	10
	b)	Explain the addressing modes of C54X with the help of examples.	10
5.	a)	What is the role of interrupt pins in a DSP device? Are these the only means of interrupting a program? How do you prevent a signal on interrupt pin from interrupting a time critical program being executed by the DSP?	10
	b)	Draw the diagram showing functional architecture of analog devices ADSP 21XX family and state its features.	10
6.	a)	Explain the implementation of FIR and IIR filters using C54X processor.	10
	b)	Draw the internal architecture of TMS 320C6X processor. Explain the functional units and their operation.	10
7.	a)	Explain the working of AIC with neat diagram.	10
	b)	What is the use of circular buffers? Write assembly language syntax in C5X for circular addressing mode? Which is the register associated with circular addressing?	10

BE | ETRX | VIII (REV) 24/5/2012
Advanced Networking Technologies

VT-EE Exam April-12-150

Con. 3980-12. **(REVISED COURSE)** **GN-7556**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Draw **neat** diagram wherever **necessary**.

1. (a) Explain TCP/IP Protocol Suite. 5
(b) Compare SONET layers with OSI or the internet layer. 5
(c) Explain ATM cell format in detail. 5
(d) What is remote monitoring ? Explain benefits of remote monitoring. 5

2. (a) Explain OSI model giving functions of each layer. 10
(b) Draw ATM protocol architecture. Explain ATM adaptation layer with respect to services and protocol. 10

3. (a) With the help of neat sketch explain DWDM. 10
(b) What do you mean by Access layer design ? Explain. 10

4. (a) Draw and explain frame format of frame relay and explain address feilds. How it provides congestion control and quality of service ? 10
(b) Explain the steps for completing the Access-Network Design in detail. 10

5. (a) Explain in detail Repeaters, Routers, Bridges and Switches. 10
(b) Explain in detail packet filtering and also mention its advantages and disadvantages. 10

6. (a) With respect to network management explain the following :– 10
(i) Documentation
(ii) OAM & P.
(b) Explain in detail network security treats. 10

7. Write short note on the following :– 20
(a) IEEE 802.11
(b) Subnetting and Supernetting
(c) Network Security Safeguard
(d) SONET Hardware.

****

29/5/2012

BE(E+TRX) Embedded System & Real time Programming 12.00 P.M. to 3.00 P.M.

Con. 4451-12. (REVISED COURSE) GN-8267

(3 Hours) [Total Marks : 100

N. B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** of the remaining **six** questions.
(3) Draw **neat** diagram and assume **suitable** data wherever **required**.

1. (a) What is H/W and S/W co-design.
(b) Explain functions of different registers available in ARM7. **5**
(c) Differentiate between Mutex, Lock () and Spinlock () inter process communications techniques with suitable example. **5**
(d) Draw and explain data frame formate of CAN bus. **5**

2. (a) Design an automatic Tea and Coffee vending machine based on FSM (Finite State Machine) Model for the following requirement the tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin the user can either select coffee or tea or press cancel to cancel the order and take back the coin. **7**
(b) Draw and explain Petrinet model. **3**
(c) Name different problems of using Semaphore, also explain priority inversion problem and its solutions. **10**

3. (a) Draw and explain status register structure of MSP430. **5**
(b) Explain different Exceptions which occur in MSP430. **5**
(c) Describe clock circuit and registers used in control it of MSP430. **10**

4. (a) Define Process, Threads and Tasks also explain various status of task. **10**
(b) What is shared data problem and mentions various methods to resolve it. (Give relevant example). **10**

5. (a) Explain Processor modes of ARM7, also specify different branch instruction used to exchange branch from ARM mode to Thumb mode. **10**
(b) Explain different addressing modes of ARM7TDMI. **10**

6. (a) Three Task with ids T1, T2, T3 with estimated time 10, 5, 7 ms and priority 1, 3, 2 resp. enters the ready Queue together. A new process T4 with estimated time 2 ms and priority 0 enters the ready queue after 2 ms. Schedule the tasks using preemptive SJF (shortest job first) and Priority based scheduling algorithm. Calculate execution time, waiting time, turnaround time, mention which is the best scheduling algorithm for a given problem. (0 is the highest priority). **10**
(b) Explain data structures Queue, Circular Queue, Linked list, Array. **10**

7. Write short notes on any **four** : **20**
(a) Explain System on chip (Soc)
(b) Spiral model used in EDLC
(c) Periodic and Aperiodic Rate Monotonic Scheduling
(d) Black box and White box testing
(e) SPI and SCI port.