BE(ETRX) SEM VIII (REV) May 2013
MMFS —
20/5/13

Con. 8544–13. **(REVISED COURSE)** **GS–3547**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. 1 is **compulsory.**
(2) Solve any **four** questions from **remaining** questions.
(3) Assume **suitable** data wherever **required.**

1. (a) Write perceptron training algorithm for several output cases. **5**
   (b) Explain Widrow-Hoff learning rule. **5**
   (c) Distinguish cross-over and mutation. **5**
   (d) What do you understand by BAM ? **5**

2. (a) Explain perceptron convergence algorithm for single layer perceptron. **10**
   (b) Compare steepest descent algorithm with LMS algorithm. **10**

3. (a) What is learning process ? What do you mean by supervised and unsupervised learning ? Explain it with suitable examples. **10**
   (b) Draw the architecture of RBFN and explain the training algorithm with fixed centres. **10**

4. (a) Explain the error back propagation algorithm with the help of flow chart. **10**
   (b) Compare RBFN and MLP in detail. **10**

5. (a) What is Hopfield model of neural network ? Explain flow energy minimization function is used in it. **10**
   (b) Explain any four defuzzification methods with suitable diagrams. **10**

6. (a) If the two fuzzy sets are given as – **10**

$$\underset{\sim}{A} = \left\{\frac{1}{2} + \frac{0\cdot5}{3} + \frac{0\cdot6}{4} + \frac{0\cdot2}{5} + \frac{0\cdot6}{6}\right\} \text{ and}$$

$$\underset{\sim}{B} = \left\{\frac{0\cdot5}{2} + \frac{0\cdot8}{3} + \frac{0\cdot4}{4} + \frac{0\cdot7}{5} + \frac{0\cdot3}{6}\right\}$$

   Find complement, union, intersection, difference and De-Morgan's law.
   (b) Explain Kohonen's self organizing learning algorithm. **10**

7. Write short notes on (any **four**) :— **20**
   (a) Types of activation functions
   (b) Properties of neural networks
   (c) Fuzzy controller to stabilize inverted pendulum
   (d) Storage and retrival in BAM
   (e) Boltzman Machine
   (f) Rate of learning.

8/05/13 BE (ETRx) Rev VIII Advance VLSI Design

55 : 1st half.13-shilpa(h)

Con. 7493-13. **(REVISED COURSE)** **GS-2965**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data wherever required and justify the **same**.

1. (a) Analog circuits design is difficult as compared to Digital circuit design. Justify. **5**
(b) Explain electromigration effect in an Inter connect. **5**
(c) Draw and explain trench capacitor and stacked capacitor structure of DRAM cell. **5**
(d) Write verilog code for 8-bit counter. **5**

2. (a) Draw the circuit using propagate and generate term for 4-bit CLA network, in **each** of the following :– **10**
(i) nFET logic
(ii) Pseudo nMos logic.
(b) Give and explain the capacitances associated with an interconnect and explain how propagation of signal depends upon the distributed RC effect. **10**

3. (a) The storage capacitor in a DRAM has a value of C_S = 55 fF. The circuitary restricts the capacitor voltage to a value of V_{max} = 3·5 V; When the access transistor is off, the leakage current of the cell is estimated to be 75 nA. **10**
(i) How many electrons can be stored on C_S ?
(ii) How many fundamental charge unit q leave the cell in 1 second due to leakage current ?
(b) Give various important parameter affecting switching performance of C MOS Inverter. Suggest methods to improve it. **10**

4. (a) Give and explain maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. **10**
(b) Implement following functions using AND-OR PLA :– **10**

$X = ac + \overline{b}c$

$Y = abc + \overline{a}\overline{b}c$

$Z = \overline{a}b + ab$

[TURN OVER

5. (a) Give and explain Interconnect scaling with its width, length, thickness and capacitances. **10**

   (b) Give and explain single phase clock system and explain its drowback. **10**

6. (a) Draw and explain C MOS two stage OP-AMP. Give gain boosting technique. **10**

   (b) Draw and explain Schmitt - trigger circuit as a input protection for C MOS. Also explain bi-directional I/O circuits. **10**

7. Write short notes on (any **three**) :– **20**

   (a) Frequency compensation scheme of CMOS Amplifier

   (b) Manchaster carry chain circuits and MODL Circuit

   (c) Pipelined system

   (d) EEP ROM Programming technique.

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BE / ETRX / VIII CREV 13/5/2013.
Robotics & Automation.

ws-Con-2013-1

Con. 8256–13. **(REVISED COURSE)** **GS–3187**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **four** questions out of the remaining **six** questions.
(3) Assume suitable data where **necessary** and justify the **same**.

Q.1 a) Define hard/fixed, soft/ flexible automation and hence the relative Cost effectiveness of different types of automation with a neat sketch. 05 marks

b) What is the different between Path & Trajectory and What is Trajectory planning? 05 marks

c) Define Pixel function, Shrink Operator and Swell operator. 06 marks

d) What are the advantages & disadvantages of PLC system. 04 marks

Q2. a) Compute the joint variable vector q = {q 1 , q 2 , q 3 , q 4 }T for the following tool configuration vector of the given SCARA robot , where w = { 203.4 , 662.7 , 557.0 , 0 , 0 , – 1.649 } ^{T} . 10 marks

b) Find the joint position of the tool tip of the Adept One robot when the joint variables are $q = [\Pi/4, -\Pi/3, 120, \Pi/2]^T$
Where $d = [877, 0.0, d3, 200]^T$ $a = [425, 375, 0.0, 0.0]^T$ 10 marks

Q3. a) Consider the Stanford manipulator, Derive the complete set of forward kinematic equations, by establishing appropriate D-H coordinate frames, constructing a table of link parameters. 15 marks

b) With neat sketch write basic four steps for transferring frame k-1 to frame k. 05 marks

Q4. a) What are the important edge detection methods for polygonal objects? Explain one of the edge detection technique? 10 marks

b) What are area descriptors? What are its advantages over line descriptors? Explain the different moments to characterizing shape? 10 marks

Q5. a) Explain how the chain code of a boundary is constructed? 05 marks

b) Consider the 8 x 10 binary image shown in Figure 1 compute the zero'th, first and second order moments , Central moments , Normalised second order moments and the principal angle of the foreground region R. 15 marks

0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	0
0	0	0	0	0	1	1	1	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 1 : A region R in 8 x 10 binary image

Q 6. a) Explain the equivalent Ladder Diagram to demonstrate De Morgan's theorem. 10 Marks.

b)Draw a ladder diagram for two motor system having the following conditions:
The start switch start motor 1; and 15 second later motor 2 starts ; the stop switch stops motor 1 and 20 seconds later motor 2 stops. 10 Marks

Q7. write short note on :
a) Classification of robots.
b) Properties of Inverse Kinematics solutions
c) Bounded Deviation Algorithm for straight line motion planning
d) Template matching technique for part recognition.

B.E (ETRX) VIII Rev 24/5/13
Embedded Syst & Real Time Prg.

96 : 1st half.13-shilpa(i)

Con. 9061-13. **(REVISED COURSE)** **GS-3808**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **four** questions out of the remaining **six** questions.
(3) Assume **suitable** data wherever **required**.

1. (a) Discuss design metric issues faced while designing an embeded system with the help of an example. **5**
   (b) Describe addressing modes of MSP 430 **OR** ARM7TDMI. **5**
   (c) Explain various basic serial communication methods. **5**
   (d) Compare software programming in assembly and C-programing lanauage. **5**

2. (a) Describe the operating modes and basic clock modules of MSP 430. **10**
   (b) Provide description of exceptions in ARM7TDMI (interrupts). **10**

3. (a) Explain thumb mode of ARM7TDMI core and compare it with normal mode. **10**
   (b) With the help of suitable (block) diagram explain :– **10**
      (i) Graphic LCD
      (ii) RS 232 /485
      (iii) PWM DC motor (speed control) interfacings.

4. (a) With the help of suitable examples, describe following C-program elements :– **10**
      (i) Header file
      (ii) Preprocessor directive
      (iii) Macro functions
      (iv) Modifier
      (v) Link-List.
   (b) For the given task calculate :– **10**
      (i) waiting time
      (ii) turnaround time for Shortest Job First (SJF) and Earliest Deadline First (EDF) scheduling. Commnet on the result. All tasks entered ready queue at same time.

Task ID	Execution Time	Deadline
T_1	06	39
T_2	16	30
T_3	18	45

[TURN OVER

5. (a) Give need for inter-process communication and synchronization. Describe the methods of the same (IPC) in detail. **10**

   (b) What is realtime system ? Compare RTOS with traditional OS. Discuss Interrupts with respect to realtime behaviour. **10**

6. (a) Design a car control embeded system with following specifications/features :– **20**

   (i) It is an electric car

   (ii) Steering angle, acceleration, direction (R/F) are inputs from driver

   (iii) It control speed, Left/Right steering, Forward/Backward direction

   (iv) Displays speed.

   For designing above system give/show –

   (1) Show block diagram for hardware

   (2) Software modules/drivers diagram, flowchart

   (3) FSM/Petrinet model of the system

   (4) Real time challenges and solutions

   (5) Suggest hardware and software solutions/tools used

   (6) Suggest testing, debugging, realtime issues.

7. Attempt any **three** :– **20**

   (a) Discuss and compare various embeded micro controller core like RISC, CISC, SOC, ARM.

   (b) Give features of CAN and explain protocol

   (c) Describe embeded programming tools like compiler, cross compiler, integrated development environment, in circuit emulator.

   (d) Explain priority inversion problems and solutions.

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BE (ETRT) SEM VIII (Rev) May 2013 20/5/13
D-SP. Proc. & Appli.

P4-RT-Exam.-Feb.-13-3-45

Con. 8837-13. **(REVISED COURSE)** **GS-3535**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Solve any **four** out of remaining **six.**
(3) Assume **suitable** data wherever **necessary.**

1. Explain briefly using appropriate diagrams wherever necessary :– **20**
   (a) Data and Program memory
   (b) Architectural differences between DSP processor and microprocessor.
   (c) Multiported memory
   (d) Special Addressing modes in P-DSP's.

2. (a) Discuss architectural features of TMS3206X. **10**
   (b) Explain what do you mean by pipeline depth and explain in what way this depth affects the pipeline performance. **10**

3. (a) What is Interpolation filter ? How can it be implemented using FIR filter ? **10**
   (b) List on-chip peripherals and their functional requirements in C5X series of digital signal processor. **10**

4. (a) Explain Interrupt Mask Register and Interrupt Flag Register of C5X. **10**
   (b) Discuss salient features of ADSP21XX series DSP processor and its functional blocks. **10**

5. (a) How does clock speed (crystal) affect the system through put in a typical controller based system ? What are the techniques used by designers to retain high through put at lower crystal speed ? **10**
   (b) What are various functional units of C54X CPU ? Explain in detail the function of compare, select and store unit (CSSU) and exponent encoder. **10**

6. (a) Discuss salient features of Motorola DSP 563XX. **10**
   (b) What are the various P-DSP families and their applications ? Discuss various factors to be considered while choosing DSP Processor. **10**

7. Write short notes on (any **two**) :– **20**
   (a) Implementation of FIR and IIR filters using C54X processor
   (b) Role of interrupt pins in a DSP device
   (c) FFT algorithm using typical DSP.
