B.E. ETRX sem VIII 3 M-2014
Sub~ ES & RTP. 31/06/14

QP Code : MV-19363

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is compulsory
(2) Answer **any three** out of remaining questions.
(3) Assume suitable data wherever required.

1. (a) Discuss design metric issues in designing an embedded system. Give suitable example. **5**

1. (b) Explain SPI protocol for serial communicaton. **5**

1. (c) Explain Operating modes of ARM7DMI. **5**

1. (d) Juistify use of C programming for embedded software development. **5**

2. (a) Explain data structure Queue, Cricular queue, Link list and Array in embedded C programming. **10**

2. (b) Explain clock circuit and registers used to control function of clock module of MSP 430. **10**

3. (a) Design an embedded system to measure frequency of a power line. Suggest hardware components used. Also give software architecture for the system. **10**

3. (b) Write ARM assembly language program to implement **10**

$$\sum_{i+1}^{N} f_i X_i \text{ for } i = 1 \text{ to } N$$

4. (a) Discuss layered architecture of CAN node. Elaborate Transfer Layer with regards to message framing and arbitration. **10**

4. (b) With the help of suitable diagram explain. **10**
(i) LCD interface
(ii) Hex Keypad interface

[TURN OVER

5. (a) What is bounded and unbounded priority inversion problem? Suggest solutions used for the same. Explain with suitable example. **10**

5. (b) For the given task table calculate: (i) Waiting time (ii) Turn around time for earliest deadline first scheduling (EDF). All tasks entered ready queue at same time. **10**

Task	Execution	Deadline
T_1	06	39
T_2	16	30
T_3	18	45

6. (a) Describe embedded programming tools like compiler, cross compiler, intergrated development environment, debugging tools, in circuit emulator. **10**

6. (b) What is shared data problem? Explain various techniques to over come shared data problem. **10**

7. Write short notes on: (**Any three**). **20**
   (i) Petrinet Modelling
   (ii) Waterfall Model in Embedded Software Development.
   (iii) Stock implementation in ARM7.
   (iv) Techniques used in Interprocess Communication in Embedded System.

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1. Elective II : Neural Networks & Fuzzy Systems

ETRX Sem VIII

22/May 2014

QP Code : **MV-19123**

(3 Hours) [Total Marks : 100

N.B. (1) Question no. **1** is **compulsory.**
(2) Solve any **four** questions from the remaining **six** questions.
(3) Assume **suitable** data wherever **required.**

1. (a) Explain different types of activation functions. 5
(b) Explain k.means of algorithm. 5
(c) Explain any two types of Defuzzification techniques. 5
(d) How many hidden layers are necessary to approximate a continuous function. 5

2. (a) Write an algorithm for back propagation training and explain about updation of weight. **10**
(b) Explain Hopfield networks in detail. **10**

3. (a) Using perceptron learning rule, find the weights required to perform following classifications. Vector (1 1 1 1) and (–1 1 –1 –1) are the members of first class. Vectors (1 1 1 –1) and (1 –1 –1 1) are the member of second class. Use two output neurons. Assume learning rate parameter as 0.9 and initial weight of 0.25. Using training vectors, test the response of net. **10**
(b) What is meant by simulated annealing. Explain procedure of Boltzman machine with its training phase. **10**

4. (a) Explain the method of solving EX-OR problem using RBF and MLP. **10**
(b) Compare supervised learning with unsupervised learning. Explain with suitable examples. **10**

5. (a) Explain the operation of fuzzy logic control with process inference block. **10**
(b) Write the properties of fuzzy set theory and explain in detail. **10**

[TURN OVER

6. (a) Three fuzzy sets are given as follows : – 10

$$\underset{\sim}{P} = \left\{\frac{0.1}{2} + \frac{0.3}{4} + \frac{0.7}{6} + \frac{0.4}{8} + \frac{0.2}{10}\right\}$$

$$\underset{\sim}{Q} = \left\{\frac{0.1}{0.1} + \frac{0.3}{0.2} + \frac{0.3}{0.3} + \frac{0.4}{0.4} + \frac{0.5}{0.5} + \frac{0.2}{0.6}\right\}$$

$$\underset{\sim}{R} = \left\{\frac{0.1}{0} + \frac{0.7}{0.5} + \frac{0.3}{1}\right\}$$

Perform the following operations over the fuzzy sets : –

(i) Max-min composition

(ii) Max product

(iii) Two corss product.

(b) Explain Kohonen's self organizing learning algorithm. 10

7. Write a short note on (any **four**) :– 20

(a) Brain state-in-a-box model

(b) Fuzzification Methods

(c) LMS algorithm

(d) Neurodynamic Model

(e) Steepest descent algorithm.

B.E. - ETRX - Sem- VII 28/5/14
Robotics & Auto.

QP Code : MV-19185

(3 Hours) **[Total Marks : 100**

NOTE: 1. Question no. one is compulsory.

2. Solve any four questions out of the remaining six questions.

3. Assume suitable data where necessary and justify the same.

Q1. (a)Explain the process of edge detection. [05]

(b)Explain programming languages used for PLC, explain any one language in brief. [05]

(c)Explain the following terms, Tool path, Tool trajectory, DOF,TCV, TWE.

[05]

(d)Write any three points why inverse kinematic solution is not unique [05]

Q2.(a)Using DH algorithm perform direct kinematic analysis of four axis ADAPT-1 SCARA robot. [10]

(b) Compute the joint variable vector $q = [q_1, q_2, q_3, q_4]^T$ for the following tool configuration vector of

SCARA. $w(q) = [692.82, 25, 527, 0, 0, -1.6487]^T$, where

$a_1 = 425mm, a_2 = 375mm, a_3 = 0, a_4 = 0$, and $d_1 = 877mm, d_2 = 0, d_3 = q_3, d_4 = 200mm.$ [10]

Q3.(a)Discuss Inverse kinematic analysis of five axis Microbot α-II Articulated Robot arm. [10]

(b) Find the composite rotation matrix by rotating the tool about the fixed axis of F frame, with a yaw of $\left(\frac{\pi}{2}\right)$, followed by a pitch of $\left(\frac{-\pi}{2}\right)$ and finally a roll of $\left(\frac{\pi}{2}\right)$ radians. If $(p)^M = (0, 0, 0.6)^T$ *Find* $[p]^F$ [10]

Q4.(a) Explain how straight line motion can be obtained using articulated robot.

[10]

(b)Differentiate between path and trajectory. Define SDF. Explain in brief how continuous motion path trajectory is generated. [10]

[TURN OVER

Q5.(a) Explain shrink and swell operators. How does swell operator help in image smoothening, explain with an example. [10]

(b)What are advantages of PLC's explain with examples, also state the specifications of PLC with Industrial application and manufacturer. [10]

Q6.(a)Compare traditional ladder diagram and PLC ladder diagram with examples. [10]

(b) Write short note on corner point detection. [10]

Q7. Write short notes on any two [20]

(a)Template matching (c) Workspace fixtures

(b)Screw transformation (d) Gross motion planning

ETRX1 Elective II DSP Processors & Architecture 22/May 2014

Sem VIII

QP Code : MV-19120

(3 Hours) **[Total Marks : 100**

NOTE- Question No. **1** is **Compulsory.**
Attempt any **Four** questions from remaining six questions.

1.	a)	Briefly explain the features of programmable DSPs to achieve high speed operations.	05
	b)	Distinguish between dual-access RAM and single-access RAM used in the on-chip memory of 5X.	05
	c)	With a block diagram explain the indirect addressing mode of TMS320C54XX processor using dual data memory operand.	05
	d)	Explain VLIW architecture with reference to TMS320C6X PDSP.	05
2.	a)	Describe the pipelining operation of TMS320C54XX processors. How pipelining increases the throughput efficiency?	10
	b)	Describe the basic features that should be provided in the DSP architecture to be used to implement the Nth order FIR filter, $y(n)= \Sigma x(i)\ h(n-i)$ where x(n) denotes the input sample, y(n) the output sample and h(i) denotes ith filter coefficient.	10
3.	a)	Explain the various registers used with ARAU and their functions.	10
	b)	Explain with the help of example, how circular addressing mode is useful in real time processing of signals. Write an assembly language program which illustrates the operation of circular addressing mode.	10
4.	a)	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	08
	b)	With an example each, explain immediate, absolute, and direct and indirect addressing modes.	12
5.	a)	Explain the following assembler directives of TMS320C54XX processors (i) .mmregs (ii) .global (iii) .include 'xx' (iv) .data (v) .end (vi) .bss	06
	b)	Explain PMST register.	08
	c)	Explain the features of ADSP-2100 processor family.	06
6.	a)	Compare the features of TMS320C5X and TMS320C54X.	10
	b)	Explain memory mapped register addressing and stack addressing in TMS320C54X.	10
7.	a)	Draw the block diagram of TMS320C62XX processor and explain its function.	10
	b)	Compare PDSPs and General purpose processors. Explain different areas of applications of DSP processors along with examples.	10

B.E Electronics sem VIII Rev. / 22 May 2014

Elective II - Adv. Networking Technologies

QP Code : MV-19117

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. 1 is compulsory.
(2) Answer **any four** from remaining questions.

1. (a) Explain the strategies for transition from IPv4 to IPv6. **20**
(b) Compare ubiquitous and hierarchical access in Access Network Design.
(c) Compare IPv4 and IPv6
(d) Explain frame format of Frame relay.

2. (a) Explain ATM cell format in detail and compare Frame velay and ATM. **10**
(b) With a neat flowchart, explain how CSMA/CA is implemented in WLAN. Why CSMA/CD cannot be implemented in WLAN. **10**

3. (a) Explain the importance of DCF, PCF, NAV vector with respect to IEEE 802.11 bringing out the importance of the protocol. **10**
(b) What are the hardware components of DWDM? Explain the technology with a neat diagram. **10**

4. (a) Explain the packet filtering and layer-7 filtering and bring out the advantages and disadvantages by comparing them. **10**
(b) Explain the functional layers of SONET and elaborate on the hardware components used in the technology. **10**

5. (a) What is a firewall? What are the capabilities and limitations of firewall? Expalin different types of firewalls with their advantages and pitfalls. **10**
(b) Explain the AAL5 layer and bring out the advantges of this layer with respect to other layers. **10**

6. (a) Explain fragmentation with respect to IPv4 and elaborate with an example. **10**
(b) With a neat sketch, elaborate the functions of OSI layer and compare it with TCP/IP layers. **10**

7. (a) Explain different security threats, mentioning the need for network security. **20**
(b) Write short notes on RMON.
(c) Explian the functions of routers, bridges and switches in networking.
(d) Explain ATM logical connections.

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Advanced VLSI Design (Rev)
BE ETRX Sem-VIII
31/5/14 11.00 to 2.00

QP Code : MV-19048

(3 Hours) **[Total Marks : 100**

N.B. : (1) Questions **No. 1** is **compulsory.**
(2) **Attempt** any **four** out of remaining **six** questions
(3) Assume any suitable data whenever required and justify the same.

1. (a) Give and explain the routing capacitance with fringing field effect. **5**
   (b) Give and explain carry save adder. **5**
   (c) Write specification of Row Decoder, Column Decoder and MUX/DMUX used in 64K X 8 SRAM. **5**
   (d) Give and explain two techniques to improve the minimum frequency requirement of clock signal. **5**

2. (a) Draw and explain full adder using dual rail complementary pass transistor logic. **10**
   (b) Give various important parameters affecting switching performance of CMOS inverter. Suggest methods to improve it. **10**

3. (a) Explain in detail sizing of routing conductor with respect to metal migration and ground bounce /power supply drop. **10**
   (b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. **10**

4. (a) Draw and explain CMOS two-stage OP-AMP. **10**
   (b) Explain various technique of clock generation. Discuss "H" tree clock distribution. **10**

5. (a) Draw three variable-three output PLA and programme it with following functions: **10**

   $fx = ac + be$
   $Fy = abc + abc$
   $Fz = ab + ab$

   (b) Give and explain interconnect scaling. **10**

6. (a) Give and explain single phase clock system and explain its drawback. **10**
   (b) Explain need of input protection and give the input protection circuits. **10**

7. Write short note on (any three) **20**
   (a) Switch Capacitor amplifier
   (b) Sense amplifier
   (c) Low power design consideration
   (d) Floating gate MOSFET.
