18/05/2018 T.E. Sem. VI CBGS
Discrete time signal processing
FFT

Q.P. CODE: 37021

Time 3 hours **Marks: 80**

N.B: (1) Questions NO.1 is compulsory.
(2) Attempt any three questions out of remaining five questions.
(3) Assume suitable data if required.
(4) Figures to the right indicate full marks.

Q 1.Solve any four 20

a. Determine the zeros of the following systems and indicate whether the system is minimum, maximum or mixed phase.

1) $H_1(z) = 6+z^{-1}+6z^{-2}$
2) $H_2(z)= 1-z^{-1}-6z^{-2}$.

b. What is multirate DSP? State its applications

c. Compare BLT and impulse invariant method.

d. Explain concept of decimation by integer D.

e. If X(K)={16,-4,0,-4}, determine x[n] using IFFT.

Q 2. a) If x(n)={ 1,2,3,} and h(n)= {1,0}

1) Find linear convolution using circular convolution.
2) Find circular convolution using DFT-IDFT. 10

b) Show the mapping from S plane to Z plane using impulse invariant method. Explain its limitations. Using this method determine H(z) if

$H(s)=\frac{2}{(s+1)(s+2)}$ if Ts=1s. 10

Q3. a) Compute DFT of sequence x(n)={ 1,2,3,4,5,6,7,8} using DIT-FFT algorithm. 10

b) Design low pass IIR Butterworth filter for following specifications

Passband attenuation =1dB

Stopband attenuation =40dB

Passband edge frequency=200Hz

Stopband edge frequency=540Hz

Sampling frequency=8KHz

Use Bilinear transformation method. 10

Q 4. a) A low pass filter is to be designed with following desired frequency response.

$Hd(e^{jw})=e^{-j2w}$ $\quad -\frac{\pi}{4} \leq w \leq \frac{\pi}{4}$

$=0$ $\quad \frac{\pi}{4} < w \leq \pi$

Determine the filter coefficients $h_d(n)$ if the window function is defined as

$w(n)=1 \quad 0 \leq n \leq 4$

$=0 \quad$ otherwise

Also determine the frequency response $H(e^{jw})$ of the designed filter. 10

b) Find DFT of $x(n)=\{1,2,3,4\}$. Using these results not otherwise find DFT

i) $x_1(n)=\{4,1,2,3\}$

ii) $x_2(n)=\{2,3,4,1\}$

iii) $x_3(n)=\{6,4,6,4\}$ 10

Q 5 a) Explain subband coding of speech signal as a application of multirate signal processing. 10

b) Determine the Direct form-I and Direct form-II realization for the system
$y(n) = -0.1y(n-1) + 0.2y(n-2) + 3x(n) + 3.6x(n-1) + 0.6x(n-2)$. 10

Q6. Write Short note on

a) Dual Tone Multifrequency Detection using Goertzel's algorithm 07

b) The effects of coefficients quantization in FIR filters. 07

c) Concept of interpolation by integer factor I 06

TE - EXTC - VI - VLSI Design - CBGS

11/06/2018

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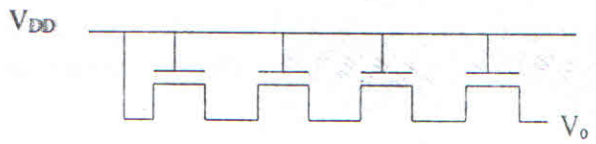
Duration: 3 Hours **Marks:80**

1] Question **no.1** is **compulsory**
2] Attempt **any three** questions out of remaining questions
3] Assume **suitable data** if **required**

Q. No. 1) **Attempt** any four from the following

a) **Calculate** the voltage at the output node V_o if V_{DD}=5V and V_{th}=1.5



b) **Implement** 2:1 multiplexer circuit using pass transistor logic and sta drawback. Draw the circuit using CMOS transmissio gates.

c) **State** the conditions required for the symmetric stati CMOS invert

d) **Compare** ion implantation with diffusion stating its a vantages and **disadvantages.**

e) **In 2-input** CMOS NAND gate all PMOS transistors have (W/L)p = NMOS transistors have (W/L)n = 10. Draw its equivalent CMOS i **simultaneous** switching of all inputs and find size of PMOS a **transistor** in the equivalent inverter circuit.

Q. No. 2)

a) A CMOS inverter has following parameters
V_{DD}= 3.3V $V_{t0,n}$= 0.6V $V_{t0,p}$ = -0.7V
K_n =200μA/V² Kp =80μA/V²
Calculate the noise margin of the circuit. Is the inverte ymmetric?

b) **Implement** $Y= \overline{A(B+C)+DE}$
(i) static CMOS logic
(ii) Dynamic logic
(iii) Depletion load logic
(iv) Pseudo NMOS logic

Q. No. 3)

a) **Explain** in detail the fabrication sequence of PMOS transistor w sectional view of each step.

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b) Draw schematic and layout diagram of six transistor SRAM cell and explain Read and write operations. [10]

Q. No. 4)

a) Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. Show the effect of scaling on power density and current density. [10]

b) Design a 3- bit carry generator block of carry look ahead adder using multiple output domino logic (MODL) style. Explain how it achieves better speed compared to ripple carry adder. [10]

Q. No. 5)

a) Draw layout diagram of two input CMOS NAND gate using lambda design Rules with $(L/W)_P=1/2$ and $(L/W)_n=2/1$. (Indicate scale in terms of lambda on layout). [10]

b) Draw transistor level CMOS negative edge triggered master slave D flip flop. [5]

c) What are the limitations of single phase clock? Explain with neat diagram two phase clock system. [5]

Q. No. 6) Write short notes on any four [20]

i) ESD protection circuit.
ii) 4x4 Barrel shifter
iii) MOSFET Capacitances
iv) Design rules and their necessity
v) Clock skew and clock jitter

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